INTRODUCTION

The world of 'Double Density' disc controllers is one that has been long in coming to the general Microcomputer marketplace. It is not without good reason. There are difficulties in data recording and retrieval encountered with this method that challenge the state of the art.

Testing a controller to respond within certain specifications is a rather straight-forward task. Being assured that similar conditions will be supplied to the controller in the field is no mean task. To make things worse the instabilities that can occur as a result of poor media (tape surface), head design and alignment, and installation environment are usually beyond the ability of most end users to detect and correct. To assist in the resolution of these possible difficulties, we have gone one step further than most of our competitors and provided additional hardware testing devices and software aids that can help point to the nature of problems. This allows efficient corrective service to be implemented.

We at Delta Products are satisfied that this advanced design controller is the finest available today. It is the result of two years of constant engineering efforts and we believe it will be the most reliable S-100 controller that can be purchased.

GENERAL DESCRIPTION

The DP-DSK is a double density, double sided disc controller which is designed to replace single density disc controllers in most S-100 applications where increased data storage capacity is needed.

CAPACITY: The DP-DSK can provide up to 4 times (1 megabyte) as much storage per diskette as a conventional single density controller. It can control up to 4 disc drives (8 heads max.) for a total on-line storage of 4 megabytes, although 2 disc drives are usually enough for most applications. Because of the increased data density, double density data transferred from diskette to user memory and from user memory to diskette is twice as fast as single density data.

COMPATIBILITY, HARDWARE: The DP-DSK will operate with a 2 MHz 8080 CPU or a 2 MHz or 4 MHz Z80 CPU with no special hardware considerations other than phantomable memory. Data transfer is accomplished via programmed I.O. methods which allow the DP-DSK to operate with all static memory and most dynamic memory. There is also an on board boot so that no system Eprom is required.

COMPATIBILITY, SOFTWARE: The DP-DSK can switch, under software or hardware control, to single density mode so that IBM 3740 compatible data can be read and written. The DP-DSK is completely compatible with CPM* in both single and double density modes.

RELIABILITY: The DP-DSK utilizes both, two level, track dependent write precompensation and a combination two phase analog-digital phase locked loop to insure reliable data transfer.

2. Open trace R on the programmable shunt with a small screwdriver.

3. Jumper pad R (directly below the programmable shunt) to one of the available Alternate I/O pins (4, 6, 8, or 24). READY will then appear on the chosen Alternate I/O pin.

RADIAL INDEX OPTION

Normally, the INDEX line from a factory configured drive is only available to the interface when the drive is selected. This option enables the user to monitor the INDEX line of each drive on the interface continuously.

Installation (refer to the PCB Jumper Locations illustration):

1. Cut trace R1 (near the center of the PCB).

2. Open trace R on the programmable shunt with a small screwdriver.

3. Jumper pad (directly below the programmable shunt) to one of the available Alternate I/O pins (4, 6, 8, or 24). READY will then appear on the chosen Alternate I/O pin.

IN USE OPTIONS

Normally, the In Use Led indicator will be energized when DRIVE SELECT is active. The door solenoid will be activated when DRIVE SELECT and READY are active. The three options listed below will energize the IN Use LED when activated to a low level.

OPTION 1

The option will energize the In Use LED when the DRIVE SELECT or IN USE line is active.

Installation (refer to the PCB Jumper Locations illustration):

Plug trace D on the optional I/O pins near connector J1.

OPTION 2

This option will energize the In Use LED when the HEAD LOAD or IN USE line is active.

Installation (refer to the PCB Jumper Locations illustration):

1. Open trace Z on the programmable shunt with a small screwdriver.

2. Plug trace D on the optional I/O pins near connector J1.

3. Plug trace Y on the optional I/O pins near connector J2.

OPTION 3

This option will energize the In Use LED only when the IN USE line is active.

Installation (refer to the PCB Jumper Locations illustration):

1. Open trace Z on the programmable shunt with a small screwdriver.

2. Plug trace D on the optional I/O pins near connector J1.

DOOR LOCK LATCH OPTION

With this option, the door lock actuator can be latched without maintaining the IN USE signal throughout the door lock interval. IN USE may be activated by DRIVE SELECT.

Installation (refer to the PCB Jumper Locations illustration):

1. Plug trace D on the optional I/O near connector J1.

2. Plug trace DL on the optional I/O pins near connector J2.

WRITE PROTECT OPTION

With this option installed, a Write Protected disk will not inhibit writing but it will be reported to the controller.

Installation (refer to the PCB Jumper Locations illustration):

Cut trace WP and jumper trace NP (located near the center of the PCB).

DISK CHANGE (ALTERNATE OUTPUT)

An active low level on this option line indicates that the READY signal has gone false (door opened) after DRIVE SELECT went false. The DISK CHANGE circuit is reset on the true to false (low/high) transition of DRIVE SELECT provided that the drive is READY. Refer to the following illustration.
Installation (refer to the PCB Jumper Locations illustration):

Plug trace DC on the optional I/O pins near connector J1.

ENGINEERING

ADVISORY

DELTA PRODUCTS

15392 Assembly Lane • Huntington Beach, CA 92649
(714) 898-1492 • TELEX 681-367 DELTMAR HTBH

Product: REV D DISK

Date: 07/13/81

Subject: MODIFICATION

File Under:

PRODUCT: REV D DISK CONTROLLER

E.A. NO. 0014

PROBLEM, SYMPTOM or PURPOSE: JUMPERING FOR DOUBLE SIDED OPERATION

AUTHOR: JIM BOSECKER

****
** **
** REV D DISK CONTROLLER JUMPER FOR DISK SELCTION **
** **
****

CONNECTOR "C2" FOR 8 INCH DRIVES "D2" FOR 5 INCH DRIVES

PIN NUM	TO	PIN NUM	JUMPER SECLETION ON DRIVE
THIS SET-UP SELECTS THE DRIVE AS A:			
4		13	DRIVE JUMPERED FOR DS1
4		12	DRIVE JUMPERED FOR DS2
4		11	DRIVE JUMPERED FOR DS3
4		10	DRIVE JUMPERED FOR DS4
FOR 5 INCH DRIVES			
1		16	DRIVE JUMPERED FOR DS1
1		15	DRIVE JUMPERED FOR DS2
1		14	DRIVE JUMPERED FOR DS3
1		13	DRIVE JUMPERED FOR DS0
THIS SET-UP SELCETS THE DRIVE AS B:			
5		13	DRIVE JUMPERED FOR DS1
5		12	DRIVE JUMPERED FOR DS2
5		11	DRIVE JUMPERED FOR DS3
5		10	DRIVE JUMPERED FOR DS4
FOR 5 INCH DRIVES			
2		16	DRIVE JUMPERED FOR DS1
2		15	DRIVE JUMPERED FOR DS2
2		14	DRIVE JUMPERED FOR DS3
2		13	DRIVE JUMPERED FOR DS0

ENGINEERING

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Product:

Date: / /

Subject:

File Under:

PRODUCT:

E.A. NO._____

PROBLEM, SYMPTOM or PURPOSE:

AUTHOR:

THIS SET-UP SELECTS THE DRIVE AS C:

6	13	DRIVE JUMPERED FOR DS1
6	12	DRIVE JUMPERED FOR DS2
6	11	DRIVE JUMPERED FOR DS3
6	10	DRIVE JUMPERED FOR DS4

FOR 5 INCH DRIVES

3	16	DRIVE JUMPERED FOR DS1
3	15	DRIVE JUMPERED FOR DS2
3	14	DRIVE JUMPERED FOR DS3
3	13	DRIVE JUMPERED FOR DS0

THIS SET-UP SELECTS THE DRIVE AS D:

7	13	DRIVE JUMPERED FOR DS1
7	12	DRIVE JUMPERED FOR DS2
7	11	DRIVE JUMPERED FOR DS3
7	10	DRIVE JUMPERED FOR DS4

FOR 5 INCH DRIVES

4	16	DRIVE JUMPERED FOR DS1
4	15	DRIVE JUMPERED FOR DS2
4	14	DRIVE JUMPERED FOR DS3
4	13	DRIVE JUMPERED FOR DS0

DRIVE SELECTION FOR 8 INCH AND 5 INCH

DRIVE SELECTION BETWEEN 8 & 5 INCH DRIVES CAN BE DONE IN ANY CONFIGURATION (EXAMPLE DRIVE A:= 5 INCH, B:= 8 INCH, C:= 5 INCH, D:= 8 INCH)

YOU MUST HAVE DELTA PRODUCTS CP/M 2.2A1 TO CORRECTLY OPERATE BETWEEN 8 & 5 INCH DRIVE.

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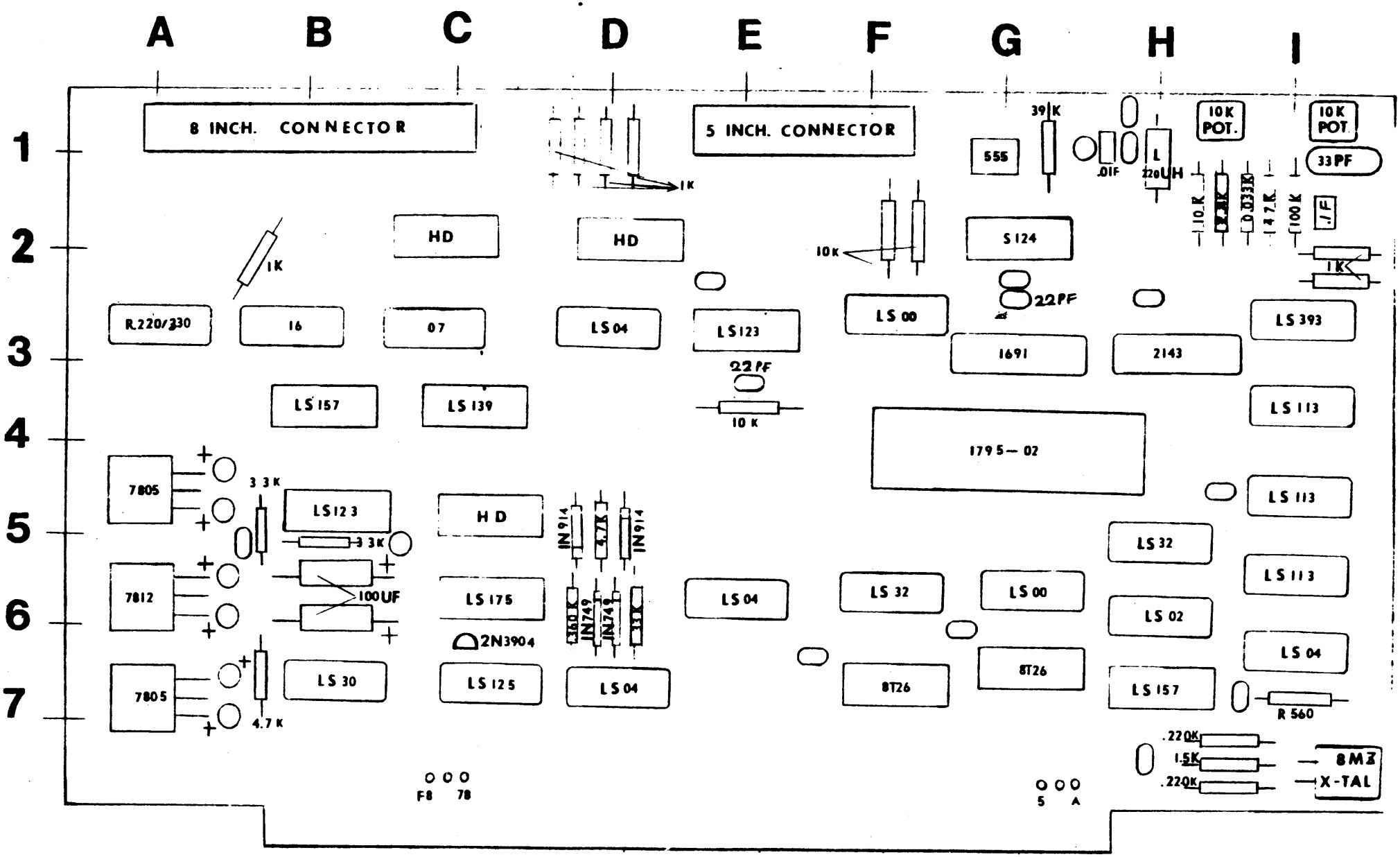
DELTA PRODUCTS

S-100 DISK CONTROLLER REV. D1



○ : 475 MT

⬭ : .1 BY CAP

PARTS LOCATING DIAGRAM

DISK UTILITIES

DTEST.COM
DFORMAT.COM
DSKTYP.COM
DFILL.COM
DFOCO.COM

DTEST.COM

The Delta Products DTEST is a quick non-destructive disk test program. Since DTEST is non-destructive it can be used to search for any bad sectors on a disk without harming data on that disk. DTEST can also be used with a known good disk to test a disk drive for read, write and interchangeability integrity.

When DTEST finds a disk error it prints the 1791 status code, the track and sector that DTEST was trying to read and the contents of the 1791 data register. DTEST then tries up to ten times to read the bad sector. If a retry is successful DTEST prints the retry number and then goes on to the next sector. If the sector could not be read in the ten retries DTEST print "11" for the retry number. This means that DTEST could not read the sector in eleven tries, DTEST then goes on to the next bad sector. When all tracks have been read by DTEST, DTEST prints the total for all the types of errors that occurred. The DTEST program can be terminated at any time by typing a 'control C'.

When DTEST is entered DTEST asks for the number of sectors per track, if the disk is single or double density and if the disk is single or double sided. The sectors per track question should be answered with a "CR" or for standard disks. (The program defaults to 26 sectors single density and 51 sectors double density.) For non standard sector sizes such as mini floppies, enter an 18 (or whatever).

> Note: When testing a double density disk, track 0 is single density, and should be tested separately as if the disk were single density. (See sample runs.)

> Note: All input and output values are in decimal except status and data, which are printed in hexadecimal.

The title line is useful when testing a box of disks or several drives. A control 'P' will tie the printer on line and ease sorting the test results later.

> Note: You should religiously test ALL media after formatting double density to insure data integrity.

```
A>DTEST


DELTA PRODUCTS DISK TEST PROGRAM 7/11/79


SECTORS PER TRACK   <CR>

SINGLE OR DOUBLE DENSITY (S,D) D
SINGLE OR DOUBLE SIDED (S,D) D

TITLE:  SAMPLE RUN OF DTEST 7/12/79        ;Optional Title

STARTING TRACK 1
ENDING TRACK 76
DRIVE NUMBER (0,1) 0
SIDE 0 OR SIDE 1 (0,1) 0
INSERT DISK AND HIT RETURN
SEEK ERRORS 0
LOST DATA 0
CRC ERRORS 0
ID ERRORS 0
OTHER ERRORS 0

TITLE:


A>DTEST


DELTA PRODUCTS DISK TEST PROGRAM 7/11/79


SECTOR PER TRACK

SINGLE OR DOUBLE DENSITY (S,D) S
SINGLE OR DOUBLE SIDED (S,D) D

TITLE:  TEST OF TRACK 0 ON A DOUBLE DENSITY DISK

STARTING TRACK 0
ENDING TRACK 0
DRIVE NUMBER (0,1) 0
SIDE 0 OR SIDE 1 (0,1) 0
INSERT DISK AND HIT RETURN
SEEK ERRORS 0
LOST DATA 0
CRC ERRORS 0
ID ERRORS 0
OTHER ERRORS 0

TITLE:  <Control C>        ;Reboot
```

DFORMAT.COM

DFORMAT program must be run on a blank disk before the disk can be used. DFORMAT program should also be run on disks that have been crashed. Be careful as this program wipes out any information you may have had on the disk.

DFORMAT writes the track and sector address I.D. fields on the disk and fills the sectors with a fill value of E5s.

In double density mode, the sector I.D. address on tracks 2-76 are written with an interleave factor of 6.

The sector I.D. addresses are written sequentially on track 1.

Track 0 is always written single density.

The last byte of the first sector on track 0 is written with a DDH instead of an E5H if the disk is to be double density. (Quad density 4DH is used.)

The DFORMAT program can format just the first to tracks of a disk (CPM tracks), so that a crashed system can be replaced without harming the rest of the data on the disk.

The MFORMAT program for mini floppy systems formats the first track single density with 18 sectors. Tracks 2 through 40 are formatted double density, 30 sector per track. The fill value is E5.

DSKTYP.COM

DSKTYP is a simple program that examines a disk and report whether it is single density, double density or quad density. To test a disk on another drive than the currently logged drive, append the letter:

```
A>DSKTYP B

                    B: is Double Density
```

DFIL.COM

The Delta Products DFILL program is used to format a disk with other than E5's as the sector fill character. This is useful in testing a disk for pattern sensitivity and for aiding in setting the precompensation values on the disk controller. DFIL is run exactly the same way as DFORMAT except DFIL asks for a fill character (in hexi-decimal). If the fill character question is answered with a 'CR' DFILL uses sequential numbers between 0 and 127 to fill all even sectors, and sequential numbers between 128 and 255 to fill all odd sectors.

DDUMP/QDUMP

DUMP

This program is an improved DUMP Utility for CP/M. Any CPM file may be DUMPED to the console in a format similar to that used by the DDT DUMP Command. In addition, any sector or group of sectors may be DUMPED in the same format. DDUMP should be used for single and double sided disks, QDUMP for Quad Density Disks.

OPERATION

The program may be run either by typing DUMP, or DUMP followed by the file name or track and sector*. If DUMP is typed the program responds with a heading followed by '*' and waits for more input. Operation in this mode is similar to other utilities like PIP or DDT.

The operation desired may then by typed in as follows:

```
DUMP FILE.NAM
DUMP A:FILE.NAM
DUMP B:FILE.NAM
```

or DUMP may be typed separately as:

```
DUMP
*FILE.NAM
*B:FILE.NAM                          (The * is a program prompt)
```

The program may also be used to DUMP disk sectors directly, DUMP any CP/M eight sector group, a map of the group allocations for the entire disk or the directory sorted alphabetically.

```
DUMP TRACK 3 SECTOR 7
DUMP TRACK 5 SECTOR 3-9
DUMP TRACK 6              (DUMPS ALL 26 SECTORS)
DUMP GROUP 19
DUMP MAP
DUMP DIR                  (DUMPS DIRECTORY)
```

The words track, sector and group may be abbreviated as follows:

```
DUMP G 4
DUMP T 7 S 3-4
*TRACK 5 S 6
*SECTOR 2-9 T 14

DUMP B: TRACK 3
DUMP A: T9 S4-6
DUMP B: G 5
DUMP B:MAP
```

Note that the format is quite free. Spaces are usually ignored. They are only required after the words track and sector or T and S, and after the word DUMP.

A limited editing feature is included in the DUMP Utility to allow changing data on the disk. The edit feature works as follows. Any single sector on either drive may be edited by requesting display of the sector followed by the EDIT.

DUMP B:TRACK 4 SECTOR 2 EDIT

The requested sector will be displayed followed by an edit prompt

EDIT –

Enter the address of the first Byte to be changed. The program will respond by typing back the address entered and the present contents of that address. To change the contents of the address enter the new Byte followed by a carriage return. The program will display the next address and its contents. To stop entering data type a period. The program will redisplay the sector showing the changes made. The edit feature works almost exactly like the S entry feature in DDT> typing only a carriage return omits entry.

Typing a period merely redisplays the sector from memory; it does not cause it to be written back on the disk. When editing is complete, redisplay the sector by typing a period and type either

WRITE	(write sector back on disk)
STOP	(stop editing without writing on disk)

All edit entries must be made in HEX. Entering non HEX characters result in an error message. The permissible address range is 0000 to 007F. Larger addresses give an error message. When entering a group of Bytes the addresses are computed Modulo 128, the next address after 007F is 0000.

The edit feature should be used with caution since it is possible to edit CP/M to "death" by changing a single Byte. One occasional valuable use is to restore files that have been accidentally erased. Erasing a file using the ERA command does not erase the data from the disk, but only enters an E5 into the first Byte of the directory. To restore a file, display the directory by displaying groups 0 and 1. Find the sector containing the name of the Byte preceding the file name from E5 to 00 and write the sector back on the disk. This will restore the file provided none of the sectors in the file were changed after the file was "erased".

An additional feature of DUMP is the ability to validate a disk.

DUMP VALIDATE
DUMP A:VALIDATE
DUMP B:VALIDATE

This causes the entire disk selected to be read one sector at a time. The sector number of any sector causing a read error will be displayed. When validating the program reads every fifth sector for speed.

As with other CP/M Utilities ^S "freezes" the display, and ^C returns to the monitor. DUMP contains many error and consistency checks. The resulting message should be self explanatory. DUMP was assembled using CP/M macro assembler, and uses a large number of macros included in a library called MACRO LIB.

DFOCO.COM

DFOCO is a fast format and copy utility for CP/M and the Delta Floppy Disk Controller. It permits formatting disks in both the standard IBM format and a variety of non-standard formats as well as copying entire disks or only specified tracks from one disk to another. In addition DFOCO permits relatively efficient single disk drive copies and will copy formats and display the format on any specified track of any disk. DFOCO supports the use of 4 disk drives.

DFOCO may be used both single density (FM) and double density (MFM). The operations performed are in general the same but may be slightly more limited in the case of double density.

DFOCO will run on any 8080 or Z-80 based system using the Delta Disk Controller. The program uses CP/M for all console input-output, however all disk operations are directly executed by DFOCO. This is necessary because DFOCO uses non CP/M commands like disk track read, and DFOCO keeps control of all disk errors to facilitate accounting and error recovery. It should be possible however, to modify DFOCO to run with any Western Digital 1771 or 1791 based disk controller. There are two different versions of DFOCO, one for standard disk drives and the other for fast seek PERSCI drives. The single density operations will be described in detail first.

SINGLE DENSITY OPERATIONS

Validating Disks

It is often useful to be able to tell whether or not the recording surface of a disk is completely intact before using the disk. This is especially true since while CP/M always checks for read errors there is no check done for write errors. You will not know you have a bad copy of a file until the first time you try to read it again which may be days or even months later.

Validating a disk consists simply of reading each sector on the disk and verifying that the CRC is correct. This simple process not only detects physical damage to the media such as scratches but also formatting errors sometimes caused by noise transients, errors which will disappear upon reformatting the disk. The following are examples of validation commands.

```
VALID                        (DEFAULT IS DRIVE A:)
VALID C:
VALID D: RETRY 20
```

The program will read the entire disk and report any read errors. If a CRC error occurs the sector will be reread a maximum of either the number of retrys specified or 10 times if no retry count is entered. Both the total number of permanent or hard error and retrys are reported at the end of the validation process.

```
SUCCESSFUL VALIDATION DRIVE B:

          OR

PERMANENT READ ERROR TRACK 17 SECTOR 5 DRIVE B
```

Copying Disks

All or part of a disk may be copied between any specified drives. The following are examples of typical copy commands:

```
COPY                                (DEFAULT IS A: TO B:)
COPY A: TO C:
COPY D: TO B: RETRY 20
COPY A: TO C: TRACK 0-1
COPY B: TO D: TRACK 3-20
COPY A: TO A:                       (SINGLE DISK TRANSFER)
```

DFOCO will respond with an acknowledgment and instructions. For example:

```
COPYING DISK A TO DISK B
TYPE RETURN TO START
```

The program will halt and wait for disks to be changed etc. and will begin the actual copy operation after return is typed. If you have made an error and wish to reenter the command type control C. The copy operation is optimized for speed. The program will determine the maximum amount of memory available and read whole tracks from the source disk until the memory is filled. Then the entire memory buffer is written onto the destination disk. All transfers are verified. As each track is written onto the destination disk it is read back and compared byte by byte with the contents of the memory buffer. Any errors are reported.

If the source and destination are the same DFOCO will first respond with a request that you verify that you really want to perform a single drive copy. If the request is acknowledged the program will indicate which disk to mount in the specified drive. As with two drive copies the program will fill the entire memory buffer with data. The program will then halt and notify you to change disks. The number of disk changes required will of course depend upon the amount of memory available. With a 48K system 8 swaps are required, with a 64K system only 6 are needed.

Copying Disks with Different Size Sectors

DFOCO will copy disks with sectors of 128, 256 or 512 bytes. The primary limitation of the program is that both disks must have the same size sectors. The size should be specified in the copy command.

```
COPY A: TO C: SIZE 256
COPY B: TO A: SIZE 512
COPY C: TO D: SIZE 128
```

Specifying a sector size of other than 128, 256 or 512 bytes will generate an error message.

Error Handling During Copy Operations

Error handling and recovery is an extremely important part of any disk file management system. DFOCO is designed to permit the maximum recovery of data from damaged or "crashed" disks. Two types of errors occur during copy operations, errors in reading from the source disk and errors writing to the destination disk. Read errors are by far the most common.

If a read error occurs DFOCO will attempt to reread the sector 10 (or retry) times. If the read error persists one of two actions may be chosen. The default is to fill the sector with E5H and write it on the destination disk. The other choice is simply to accept the data as read in and write it on the destination disk. This is the nofill option. Nofill permits the maximum data recovery but requires careful inspection of the sector causing the error since the errors may not be obvious.

Write errors are handled in a somewhat different fashion. Since there is usually no valuable data on the destination disk, the normal choice is to not permit copy operations if write error occur. DFOCO will attempt to write a sector 10 (or retry) times. If the error persists, DFOCO will stop the copy operation and validate the destination disk thus reporting all bad sectors. It is possible to copy in the presence of write errors by turning off the write verification, the noverify option. However since disks have become relatively inexpensive this option is probably unwise except in very special cases. Some examples are as follows:

```
COPY B: TO C: NOFILL RETRY 25
COPY A: TO B: TRACK 0-5 NOVERIFY
COPY D: TO A: NOVERIFY NOFILL
```

Disk Formatting and Mapping

The standard IBM format for 8 inch floppy disks is given in the Western Digital Documentation for the 1791 disk controller chip and in various IBM documents. The usual format is "soft sectored". This means essentially that the track and sector numbers are actually written on the disk as data rather than being determined by the presence of physical indicators such as holes in the disk. Formatting a disk consists of writing both the track and sector numbers as well as clocking information for the controller on the disk. It is important to remember that a "blank" disk is by no means really blank. Rather it contains a great deal of formatting information without which the controller is totally unable to read it.

Because of this "soft sectoring" it is sometimes possible and often useful to change the format to allow increased amounts of data to be written on the disk or higher speed of operation. There are two possible changes that are useful, changing the size of the sectors or changing their ordering.

This version of DFOCO supports three different sector sizes using the "IBM" soft sector format. Sectors may be formatted with the normal 26 sectors of 128 bytes or with 16 sectors of 256 bytes or 8 sectors of 512 bytes each. Using 256 or 512 byte sectors allows approximately 20% more data to be written on a single disk, however there are at present few programs which will support the use of larger sectors. DFOCO also supports a wide variety of sector orderings.

The design of CP/M dates from a time when disk controllers were quite slow and computer memories small and very costly. Small memories dictated small sector sizes on disks since the larger the sectors the larger the memory buffers required. Slow controllers meant that having read a sector from the disk it was necessary to wait before another sector could be read. Delays of 5 sector times (about 25 msec) were common. Thus CP/M is set up to read every 6th sector around the disk. This strategy unfortunately is far from optimal for present day controllers which can read consecutive sectors from a disk with ease. Note that DFOCO which reads an entire track in a single disk revolution is over 5 times as fast as PIP. Unfortunately CP/M standard system programs such as PIP and the assembler can only be speeded up a small amount, about 20 percent, by changing disk formats alone. However, new programs written to take advantage of faster controllers can be speeded up a great deal more.

Mapping Disk Formats

When experimenting with nonstandard formats it is often very useful to be able to read and display the actual disk format. You can't necessarily tell what's on a disk by looking at the label. The map command reads the format from a single track on a specified disk and displays it. There are 26 sectors per track in the standard IBM format which are numbered in sequential order. To display the sector ordering type:

```
MAP                                  (DEFAULT IS TRACK 0 DRIVE A:)
MAP C: TRACK 76
```

The program will read the specified track and display the physical to logical sector mapping. The physical sectors starting from the single index hole in the disk are simply numbered 1 thru 26. The corresponding logical sectors actually written on the disk are displayed beside the physical sector number. For disks formatted with less than 26 sectors, the unused logical sector numbers display as a '-'.

Occasionally DFOCO will display obviously incorrect mapping data, for example track 404 sector number 201. This means the format on the disk is incorrect. The disk controller will often read these disks correctly but it is usually a good idea to copy the data to a correctly formatted disk. Formatting problems of this type often show up when you attempt to read disks produced on another computer system. If the head alignment is only slightly different from yours you may get mapping errors even though you are usually able to read the data correctly.

Formatting Disks

DFOCO permits formatting disks on any drive supported by CP/M. Either the entire disk or specified tracks may be formatted. It is even possible to write different formats on different tracks of the same disk.

Standard Format

To write the standard IBM format on a disk type:

```
FORMAT                               (DEFAULT IS DRIVE A)
FORMAT B:
FORMAT C: TRACK 20-40
```

The program will halt and then respond with:

```
STANDARD IBM 3740 FORMAT

INSERT DISK TO BE FORMATTED IN DRIVE A
TYPE CARRIAGE RETURN
```

Non-standard formats may have almost any form you specify. The first variation is to offset the same format from track to track. This is useful to compensate for the time it takes to step the head from one track to another and is one of the techniques used in DFOCO to increase the copy speed. The following is an example of track offsetting:

```
FORMAT B: OFFSET 5
```

This results in the following format on the disk:

	TRACK 0	TRACK 1	TRACK 2	ETC.
SECTOR	1	6	11	
SECTOR	2	7	12	
SECTOR	3	8	13	
SECTOR	4	9	14	

A second formatting variation is to skew the sectors by a constant amount. This can be specified as follows:

FORMAT B: SKEW 3

This will result in a display of the physical to logical sector mapping and permit changing the specifications before writing the format on the disk.

PHYSICAL SECTOR	LOGICAL SECTOR	PHYSICAL SECTOR	LOGICAL SECTOR
1	1	14	14
2	4	15	17
3	7	16	20
4	10	17	23
5	13	18	26
6	16	19	3
7	19	20	6
8	22	21	9
9	25	22	12
10	2	23	15
11	5	24	18
12	8	25	21
13	11	26	24

Type return to format, sector no to correct.

Typing a sector number allows the logical sector number to be changed. Before using a sector number it must be first set to zero since the program checks and does not permit two sectors with the same number. The sector mapping is redisplayed for verification after each change.

The final formatting option is simply to type in the physical to logical sector mapping for each sector. To select this option type:

SPECIAL FORMAT A:

The program will respond by displaying each physical sector number and waiting for the corresponding logical sector number to be entered. Again the program checks the sector numbers as entered and will not allow the same sector number to be used twice.

Note that the various options may be combined if desired.

SPECIAL FORMAT B: TRACK 0-1
FORMAT C: OFFSET 6 SKEW 3 TRACK 10-76

It is even possible to copy the format from one disk to another

```
COPY FORMAT A: TO B:
COPY FORMAT B: TO D: TRACK 10
```

Formatting with Different Size Sectors

The default sector size generated by DFOCO is 128 bytes, however the program will also format tracks with 16 sectors of 256 bytes or 8 sectors of 512 bytes. The sector size is specified by the size parameter.

```
FORMAT B: SIZE 512
SPECIAL FORMAT A: SIZE 256
FORMAT C: OFFSET 2 SIZE 512
```

Caution must be used with the special format option since DFOCO will allow sector numbers greater than the number of sectors on a track. The 1791 will actually read sectors numbered in this fashion. For example a track may be formatted with 8 512 byte sectors numbered 11 thru 18, however disks written in this fashion may not validate correctly. It is also possible to format a disk with different size sectors on different tracks. Again, disks written in this fashion may not validate correctly.

Regardless of the sector size and mapping chosen, track 0 of the disk is always written in the standard IBM 3740 format. This is done to facilitate identification of the disk format by a program. Read and write operations to a disk may actually be impossible and "hang" the controller if the program expects a format that is not present. This is especially true if the incorrect density is selected.

Program Timing

The following timing figures are typical of a 64K system and will be slightly higher for smaller systems. The copy timings vary with disk formats. If the format is non-standard but the same on both disks the times are the same as for standard formats but if the sector formats are different on the two disks the copy times will be increased. The following timings are for single density only.

VALIDATING	17 SEC
FORMATTING	43 SEC (INCLUDES VALIDATION)
COPY SAME FORMAT	46 SEC
COPY DIFFERENT FORMAT	90 SEC AVERAGE
	300 SEC WORST CASE

If the format is different on different tracks of a disk it may be possible to increase copy speed with the using option. Since a write operation takes twice as long as a read operation the program can optimize the copy by reading the track format from the destination disk and using it to control reading and writing. A sample copy with this option is:

```
COPY A: TO B: USING 3
```

This causes track 3 to be read from the destination disk and used to control the copy operation. This can often double the copy speed if the formats are different on the two disks.

DOUBLE DENSITY OPERATIONS

With a few exceptions the same operations are available double density as are available single density. Double density may be selected either by adding a D to the desired command or by placing the code DD anywhere on the command line. Some examples:

```
DVALID B:
VALID A: SIZE 512 DD

DCOPY A: TO B: SIZE 256
DCOPY
COPY B: TO D: DD SIZE 512

DFORMAT
DFORMAT B: SIZE 512
FORMAT C: SIZE 256 DD
```

The following exceptions should be noted. The mapping function is not available double density. It is difficult to do an accurate track read of the format on a double density disk due to the format used. Even where not specifically prohibited, it is recommended that operations requiring track read such as copy format or copy using not be attempted. Problems in reading the format from disks may cause unpredictable results.

The special format function is not available double density. The standard formats provided by the program double density are as follows:

128 BYTE SECTORS –

Track 0 standard 3740 format single density. Tracks 1-76 have 51 sectors written in a 6 to 1 interlace pattern for use with CP/M vers 1.4. The sector order is as follows:

```
1,18,35,10,27,44,2,19,36,11,28,45,3,20,37,12,29,46,4,21,38,13,30,47,5,
22,39,14,31,48,6,23,40,15,32,49,7,24,41,16,33,50,8,25,42,17,34,51,9,26,43
```

One additional feature is provided for use with CP/M. The last byte of data on track zero sector one is written with a special flag byte to indicate the format of the rest of the disk. The codes are

```
E5      SINGLE DENSITY (E5 IS THE STANDARD FILL CHAR)
DD      DOUBLE DENSITY 51 SECTORS PER TRACK
4D      "QUAD" DOUBLE DENSITY  DOUBLE SIDED DISK
```

To insert the "QUAD" code into sector one of a 128 byte sector disk the following examples may be used:

```
DFORMAT C: QUAD
DFORMAT A: QUAD
```

256 Byte Sectors –

Double density disks formatted with 256 byte sectors are in standard IBM format. 26 sectors of 256 bytes. Track zero is single density 3740 format. There is no flag byte in sector 1 of track zero.

512 Byte Sectors –

Double density disks formatted with 512 byte sectors have 16 sectors per track. Track zero is standard 3740 format. No flag byte on track zero.

The offset and skew functions work as before although the effect of further skewing the already interlaced 128 byte pattern may be confusing.

Copying disks double density is almost exactly the same as copying them single density. Two simple rules must be observed.

1. Both disks must be of the same density.
2. Both disks must have the same sector size.

A violation of these rules may cause the controller to "hang" requiring the computer to be reset to recover.

It will be noted that copy operations on double density disks having 51 sectors is much slower than other copy operations. This is because the sectors on these disks are written so close together that the 1791 controller does not have time to write consecutive sectors although it is able to read consecutive sectors in this format. Copy operations on disks in this format read and write every other sector thus requiring twice as many disk revolutions and twice the time.

Double sided or "quad" disks are not automatically copied by DFOCO in a single operation but require two copy operations. To copy a "quad" disk you might type:

```
DCOPY A: TO C:          (COPY THE FRONT SIDE)
DCOPY B: TO D:          (COPY THE BACK SIDE)
```

A single "quad" copy operation will be added to DFOCO later.

FILE NAMING CONVENTIONS

The master BIOS from which all other BIOS's are created is:

DBIOS.ASM

For the boot:

DBOOT.ASM

and for the format programs:

FORMAT.ASM

To make a hex file of one of the above programs, first type the master ASM file to see if the equates and memory size are set the way you want. If not edit the file.

When all the equates are set assemble the file and rename the newly created hex file to a new name – as follows:

For DBIOS:

Quad Density (Double Sided Double Density) –	QBIOSXX.HEX
Double Density Single Sided –	DBIOSXX.HEX
Mini Quad Density –	MQBIOSXX.HEX
Mini Double Density Single Sided –	MDBIOSXX.HEX

For DBOOT:

Double Density Disks –	DBOOTXX.HEX
Single Density Disks –	SBOOTXX.HEX
Mini Double Density –	MDBOOTXX.HEX
Mini Single Density –	MSBOOTXX.HEX

For format (Single and Double Density):

8 inch flops –	DFORMAT.HEX
5 inch flops –	MFORMAT.HEX

Renaming only the hex files insures that any changes made to the master file are incorporated in all possible other versions of that file.

The equates in the DBIOS are:

Quad Density– dual headed drives only!

DBLSID	=	True
MINI	=	False for 8 inch; true for 5 inch drives
DUAL	=	False

WESTERN DIGITAL
CORPORATION

FD176X-02
FLOPPY DISK FORMATTER/CONTROLLER FAMILY

FEATURES

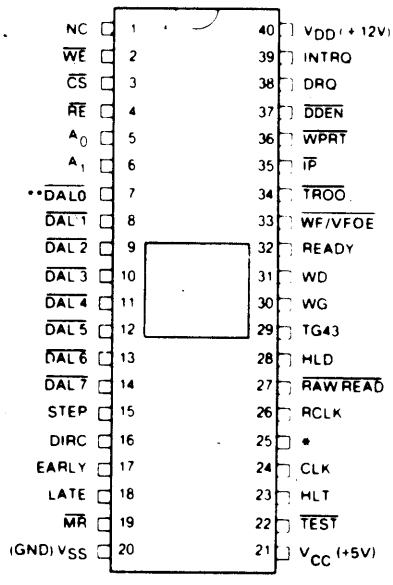
- 1 MHZ VERSION OF FD179X
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY

176X-02 FAMILY CHARACTERISTICS

FEATURES	1761	1763	1765	1767
Single Density (FM)	•	•	•	•
Double Density (MFM)	•	•	•	•
True Data Bus		•		•
Inverted Data Bus	•		•	
Write Precomp	•	•	•	•
Side Selection Output			•	•

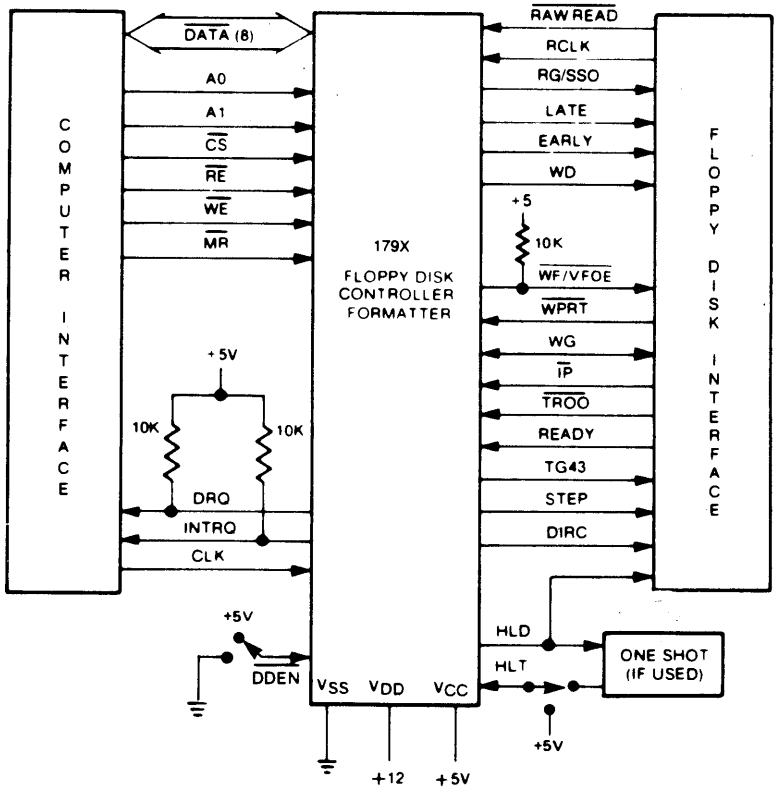
APPLICATIONS

5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY CONTROLLER/FORMATTER



*1761/3 = RG;1765/7 = SSO
**1763/7 TRUE BUS

PIN CONNECTIONS



FD176X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 1 MHZ ± 1% 50% duty cycle square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1761, 1763)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1765, 1767)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 400 ns (MFM) or 1000 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1765/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1761/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD176X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	$\overline{IP}$	This input informs the FD176X when the index hole is encountered on the diskette.
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.

GENERAL DESCRIPTION

The FD176X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD176X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD176X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD176X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD176X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD176X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1763 is identical to the 1761 except the DAL lines are TRUE for systems that utilize true data busses.

The 1765/7 has a side select output for controlling double sided drives.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

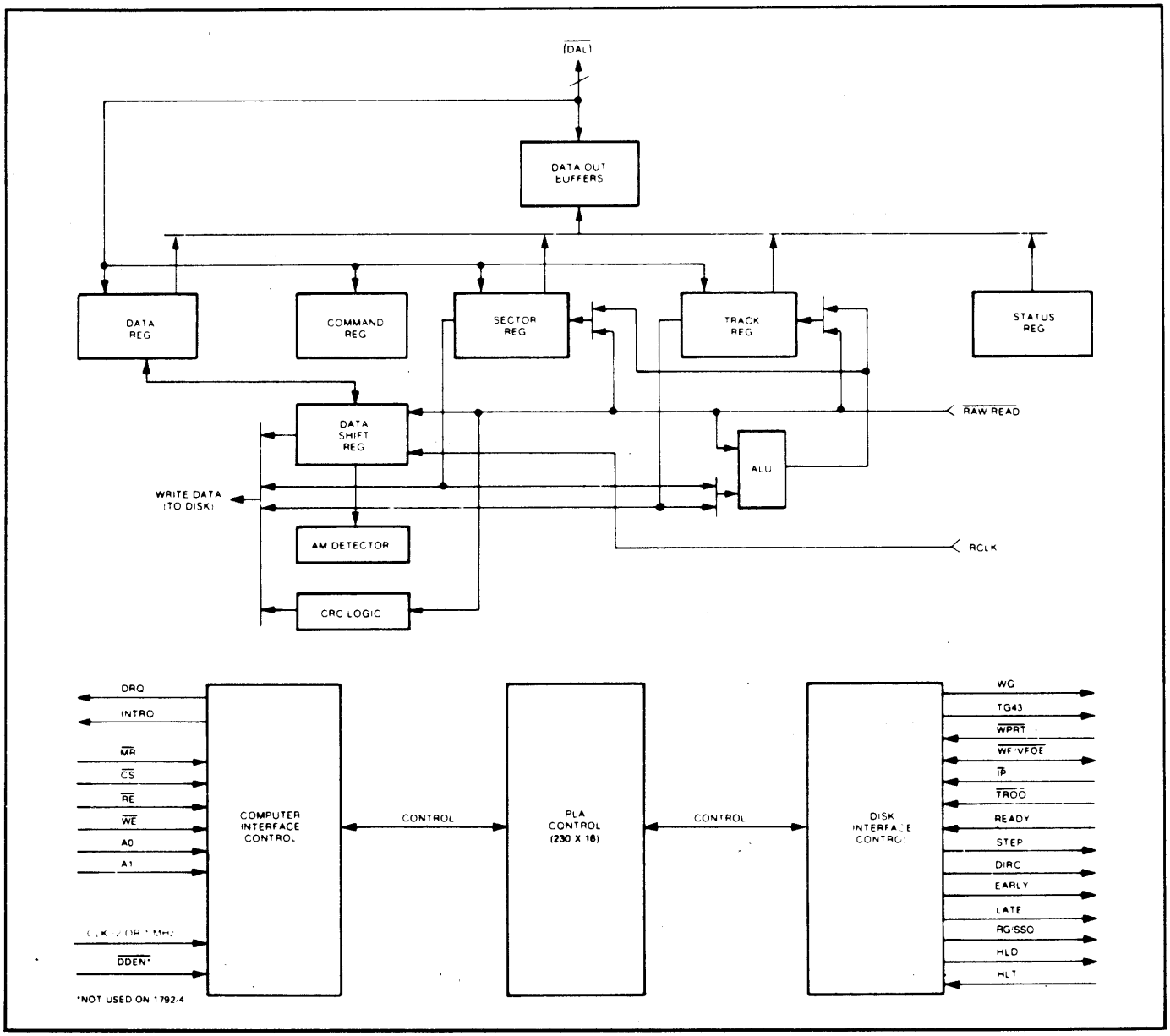
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD176X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double



FD176X BLOCK DIAGRAM

density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD176X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD176X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 176X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 1 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1765/67 may vary — see command summary.

The number of sectors per track as far as the FD176X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD176X is concerned is from 0 to 255 tracks.

For read operations in 5¼" double density the FD176X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 400 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1761/63 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD176X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD176X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD176X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 176X is inspecting data off the disk

If $\overline{WF/VFOE}$ is not used, this pin may be left open, as it has an internal pull-up resistor.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD176X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD176X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD176X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 1000 ns pulses in FM ($\overline{DDEN}$ = 1) and 400 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) an LATE (Pin 18). EARLY is active true when the WD puls appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD176X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD176X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD176X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is se When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1761, 1763

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	I_1	I_3	I_2	I_1	I_0

B. Commands for Models: 1765, 1767

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Load head at beginning h = 1, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 30 MS Delay	E = 0, No 30 MS delay E = 1, 30 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	

	LSB's Sector Length in ID Field 00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_1 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 4 μs (MFM) or 8 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

$\overline{DDEN}$	0	1	x
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0
0 0	6 ms	6 ms	368μs
0 1	12 ms	12 ms	380μs
1 0	20 ms	20 ms	396μs
1 1	30 ms	30 ms	416μs

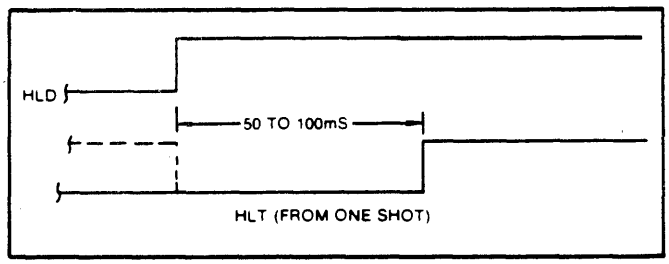
After the last directional step an additional 30 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 30 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD176X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD176X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD176X which is used for the head engage time. When HLT = 1, the FD176X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire one shot. The output of the one shot is then used for HLT and supplied as an input to the FD176X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD176X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 30 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 30 ms occurs, and the FD176X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 30 ms delay occurs and the FD176X then wait for HLT to occur.

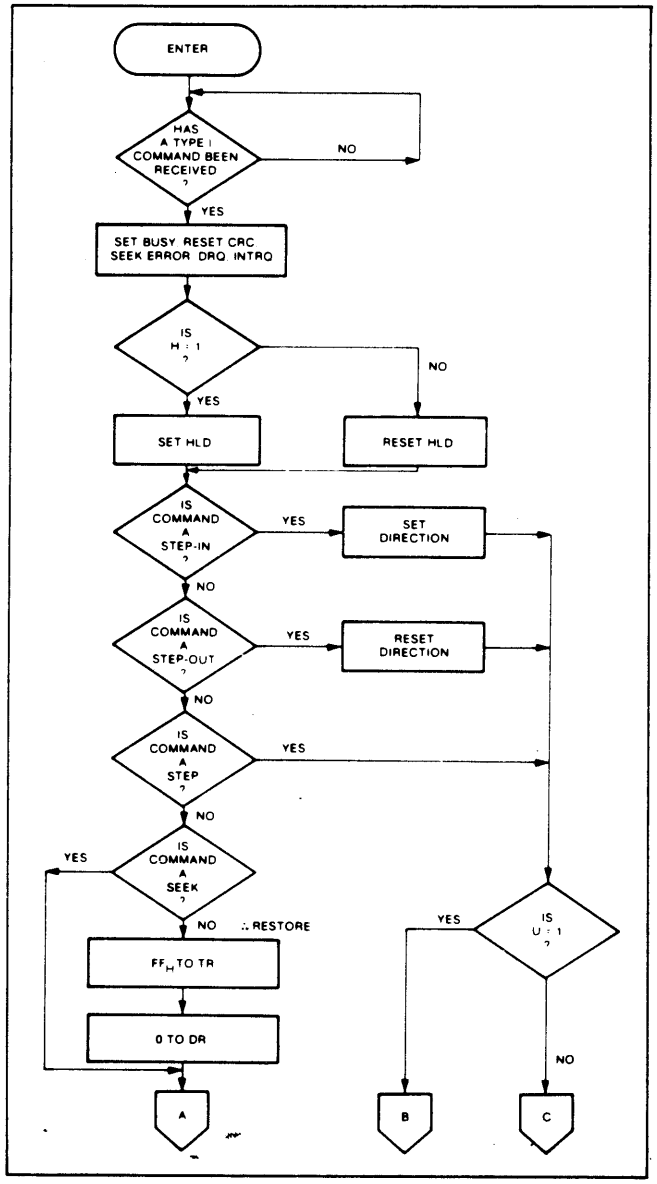
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 30 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

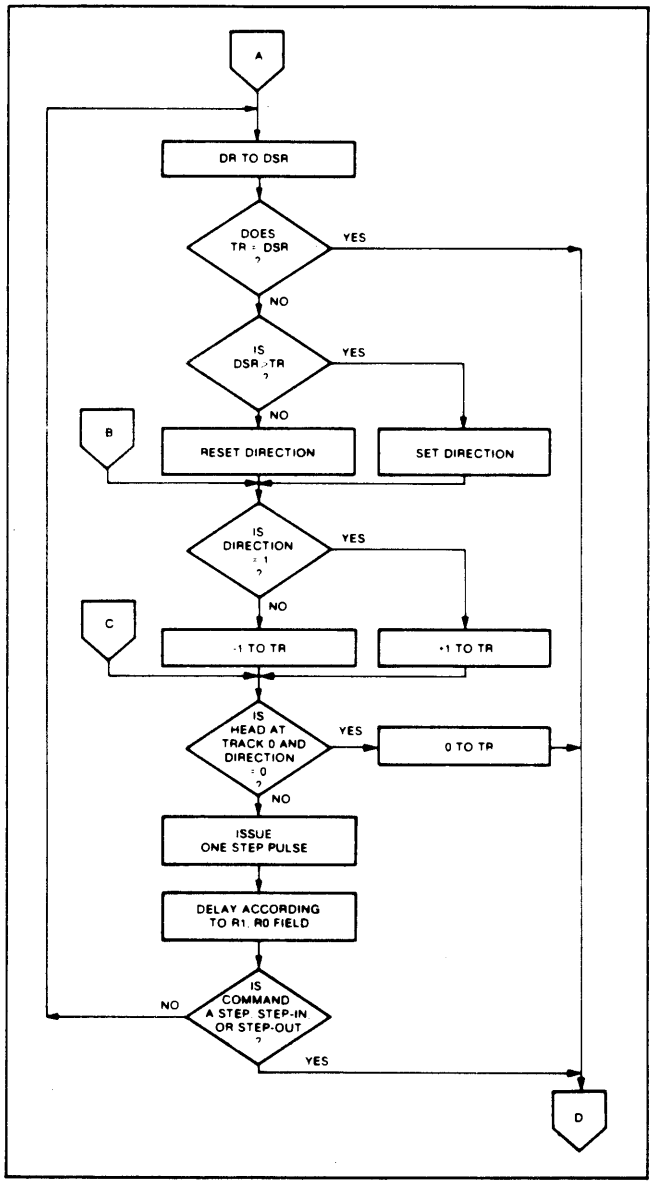
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD176X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD176X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD176X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD176X issues one stepping pulse in the direction towards track 80. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

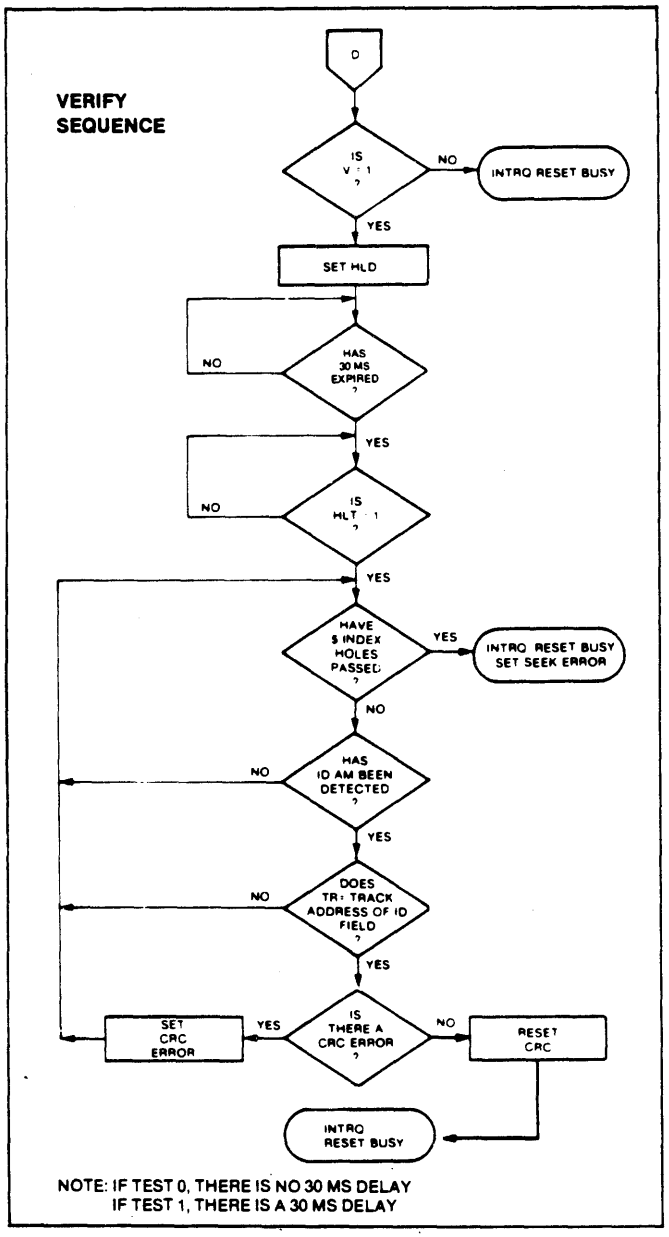
Upon receipt of this command, the FD176X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1765/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

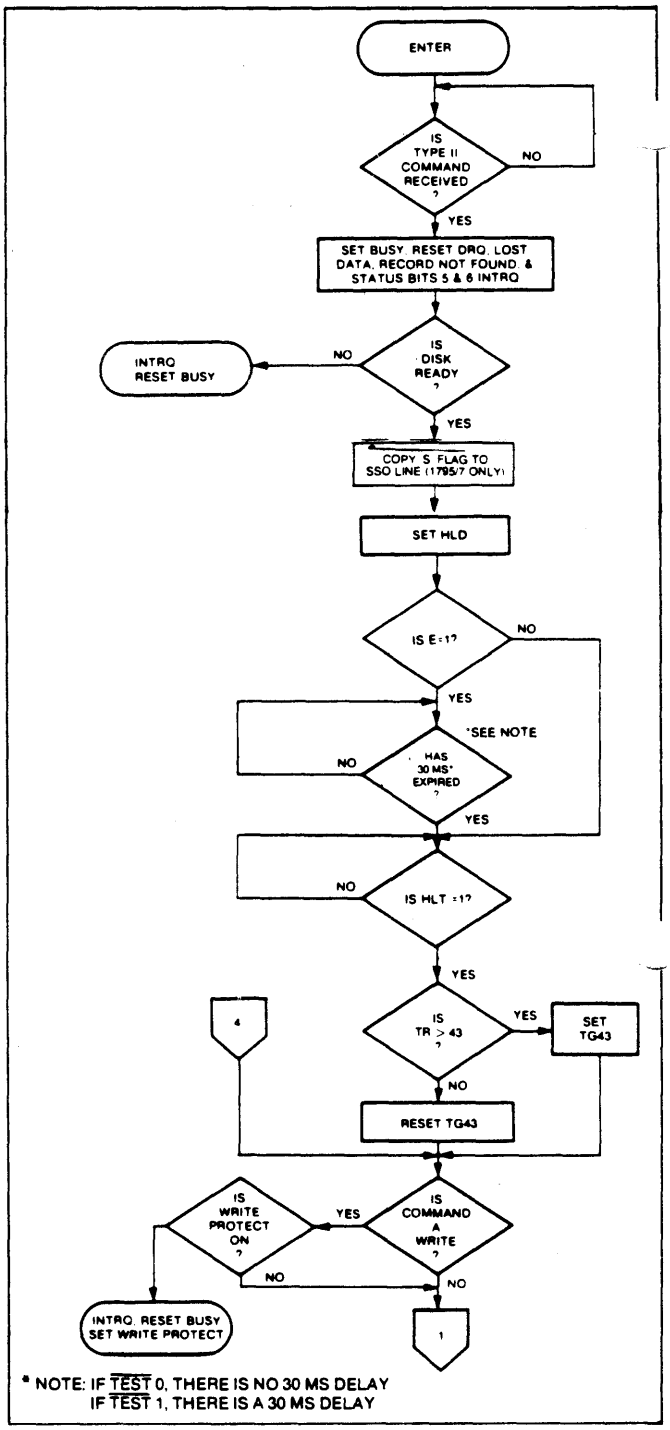
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command



TYPE I COMMAND FLOW

into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 30 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 30 msec delay. The ID field and Data Field format are shown on page 16.

When an ID field is located on the disk, the FD176X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD176X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the



TYPE II COMMAND

Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at t' completion of the command. If m = 1, multiple records a read or written with the sector register internally updated so that an address verification can occur on the next record. The FD176X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the

number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD176X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD176X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1761-63 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD176X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

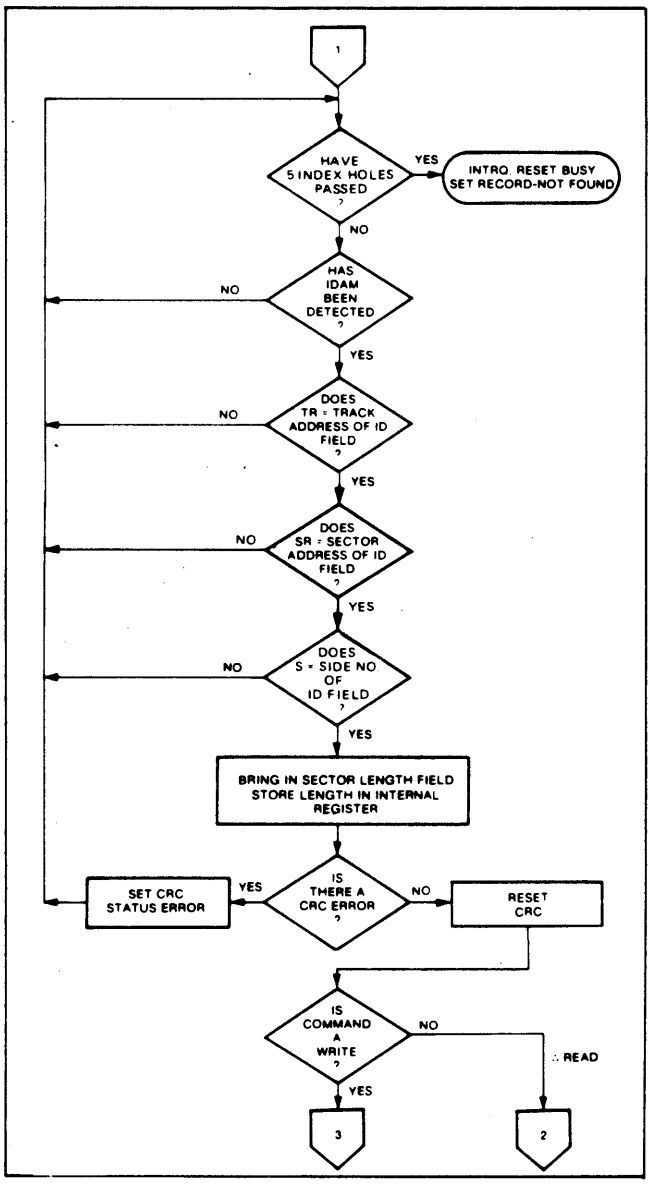
The Type II and III commands for the 1765-67 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 1765/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

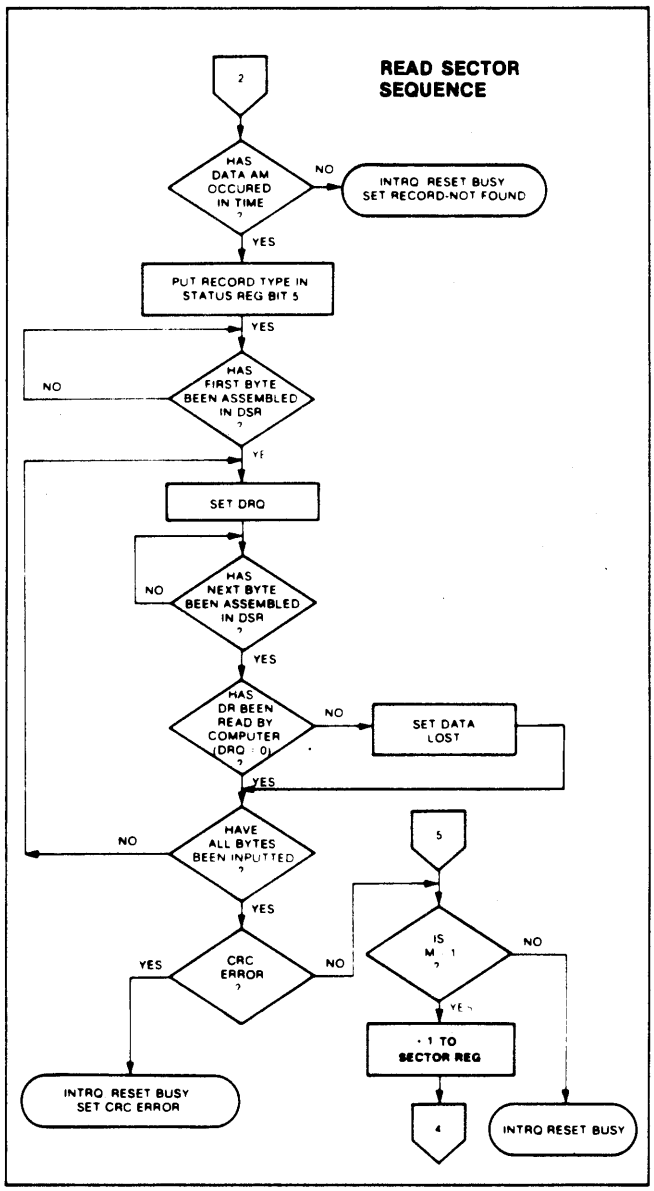
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

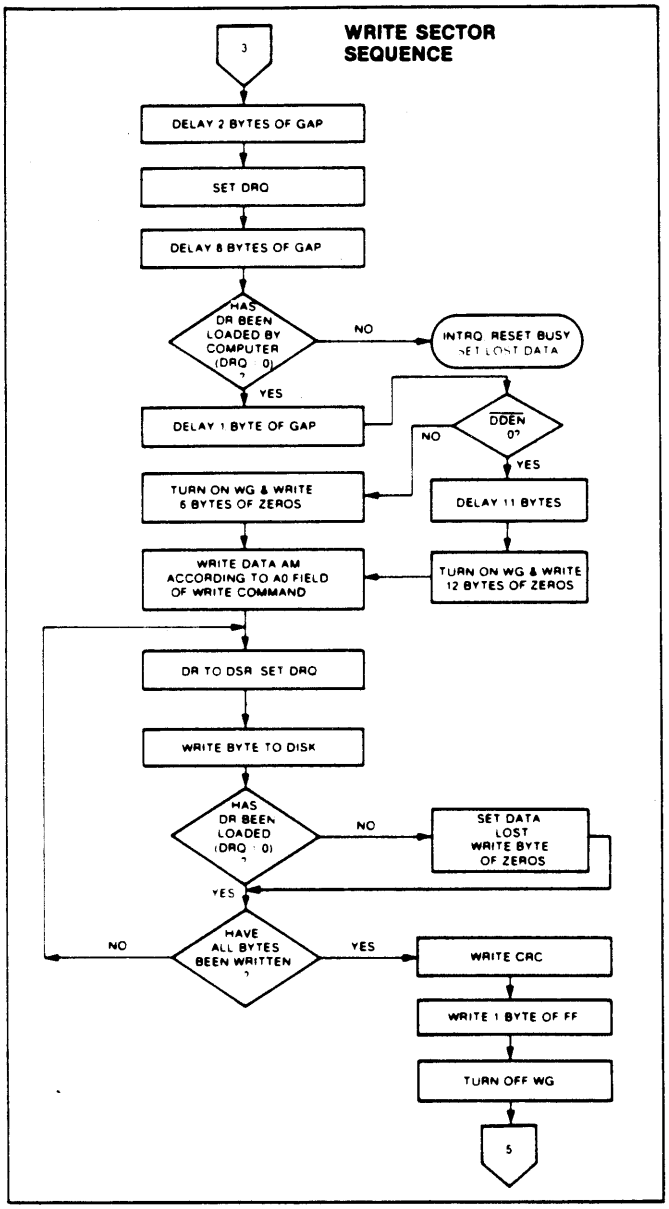
When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in



TYPE II COMMAND



TYPE II COMMAND



TYPE II COMMAND

the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD176X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD176X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk.* The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 1 MHz clock the INTRQ will set 16 to 24 μsec after the last CRC byte is written.

*If partial sectors are to be written, the proper method is to write the data and fill the balance of the sector with zeroes. Do not let the chip supply the filler by not servicing the DRQs. Doing this will mask any errors by the lost data status and the CRC's may be incorrect.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD176X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark

encountered. An interrupt is generated at the completion of the command.

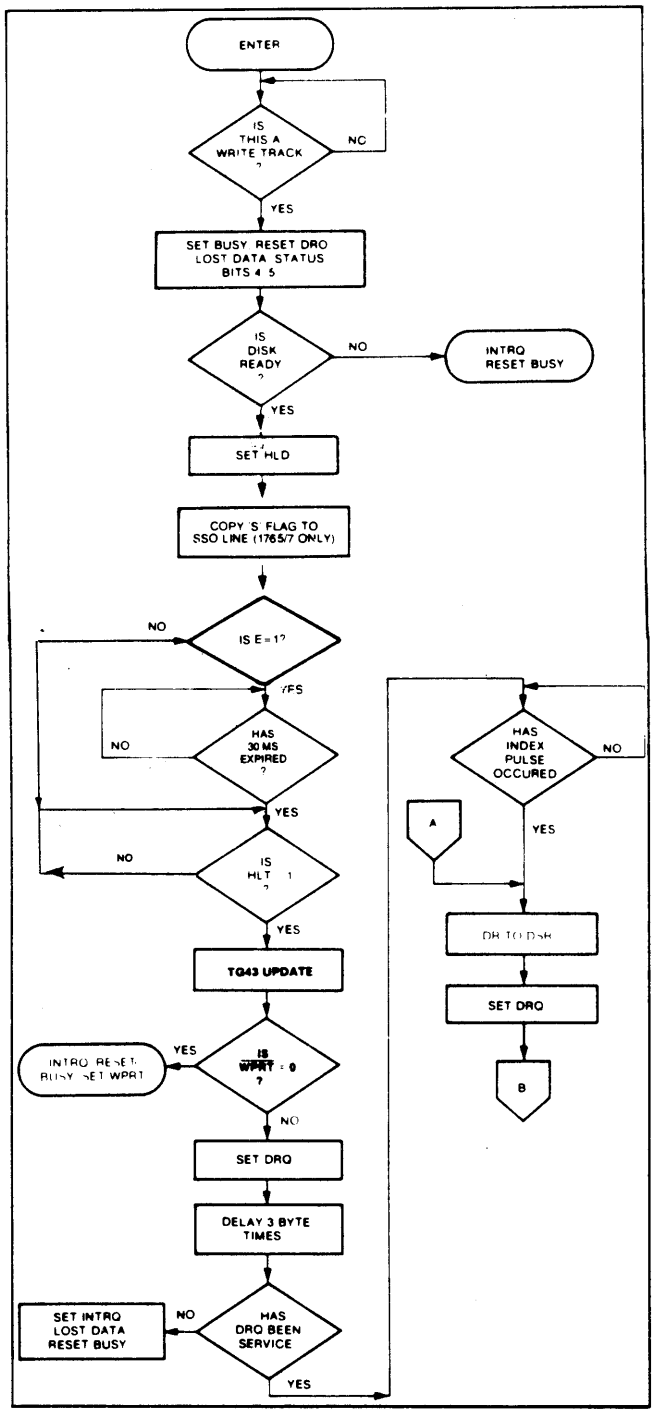
This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

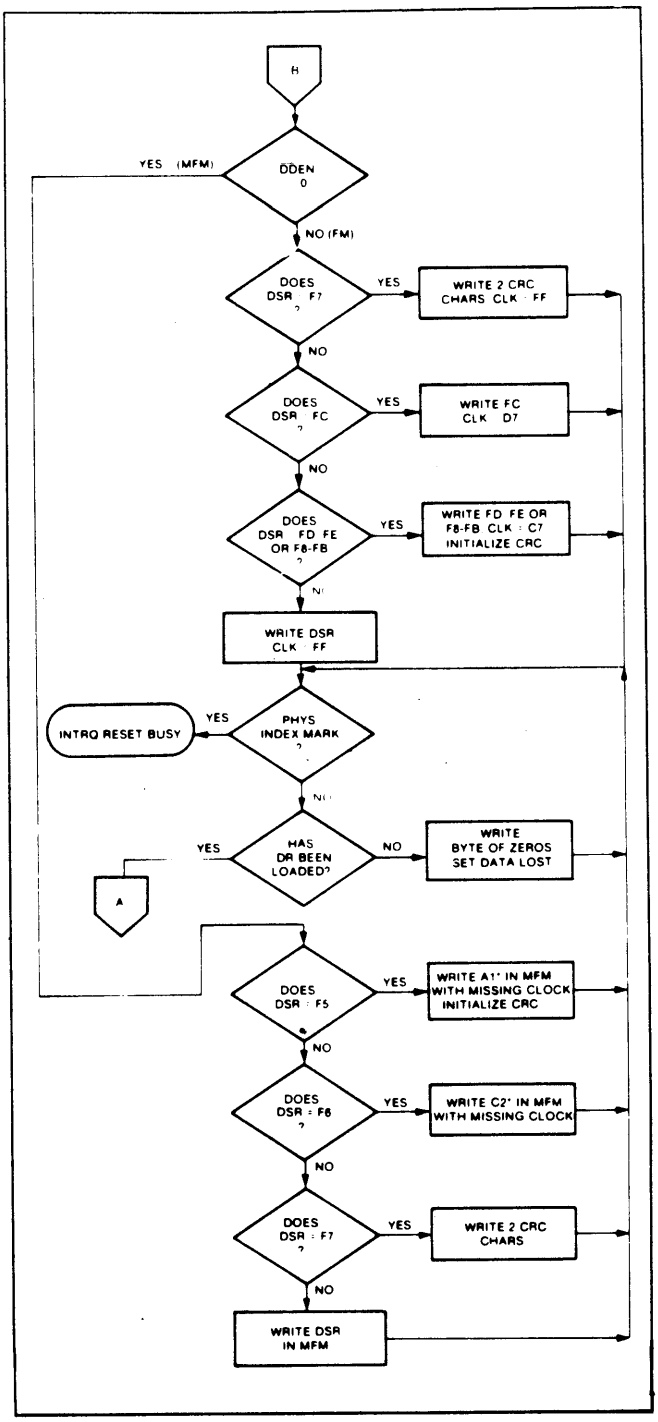
The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the





CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD176X INTERPRETATION IN FM (DDEN = 1)	FD176X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted. See note on page 12.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD176X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

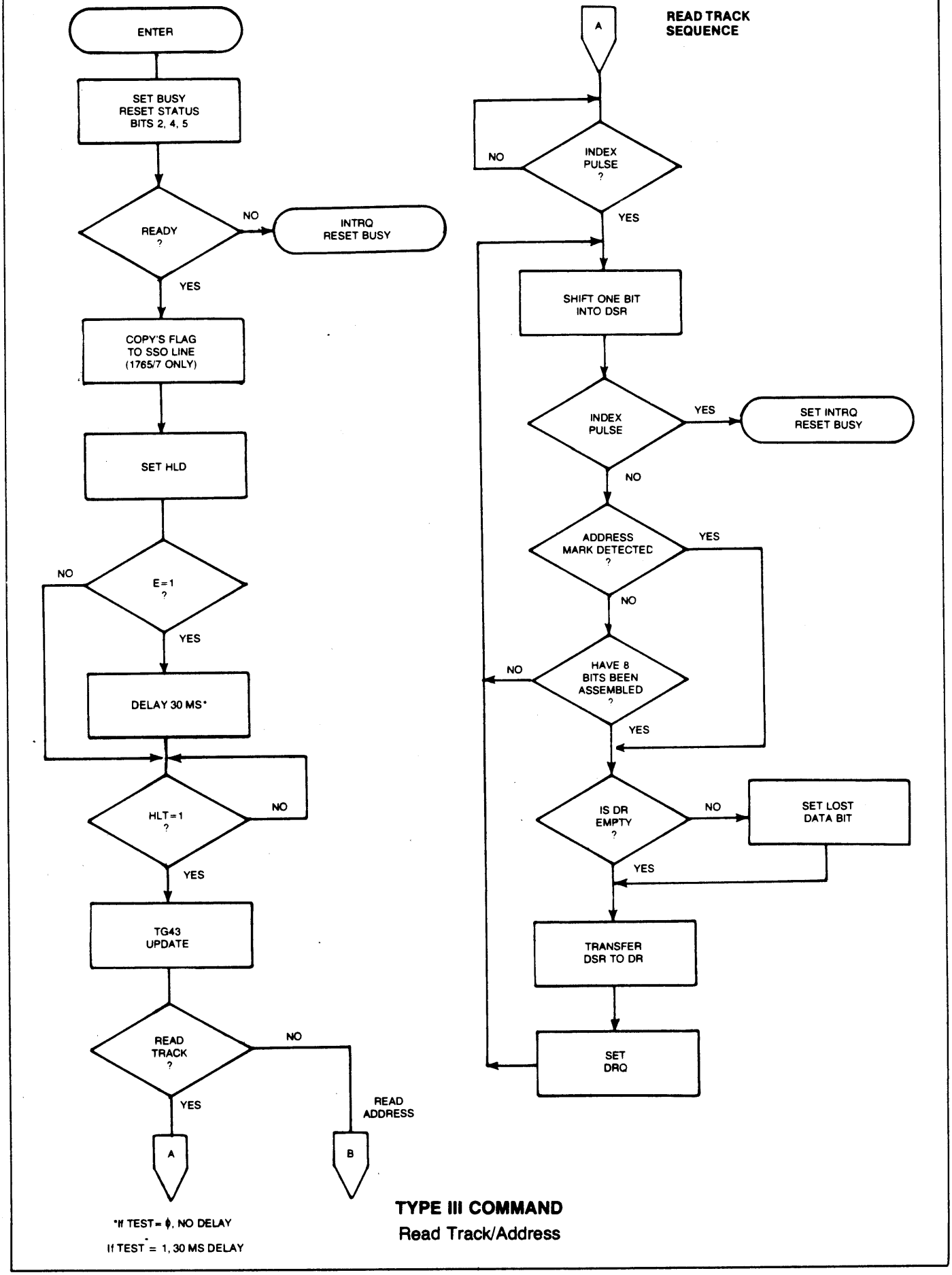
Wait 16 micro sec (double density) or 32 micro sec (single density before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

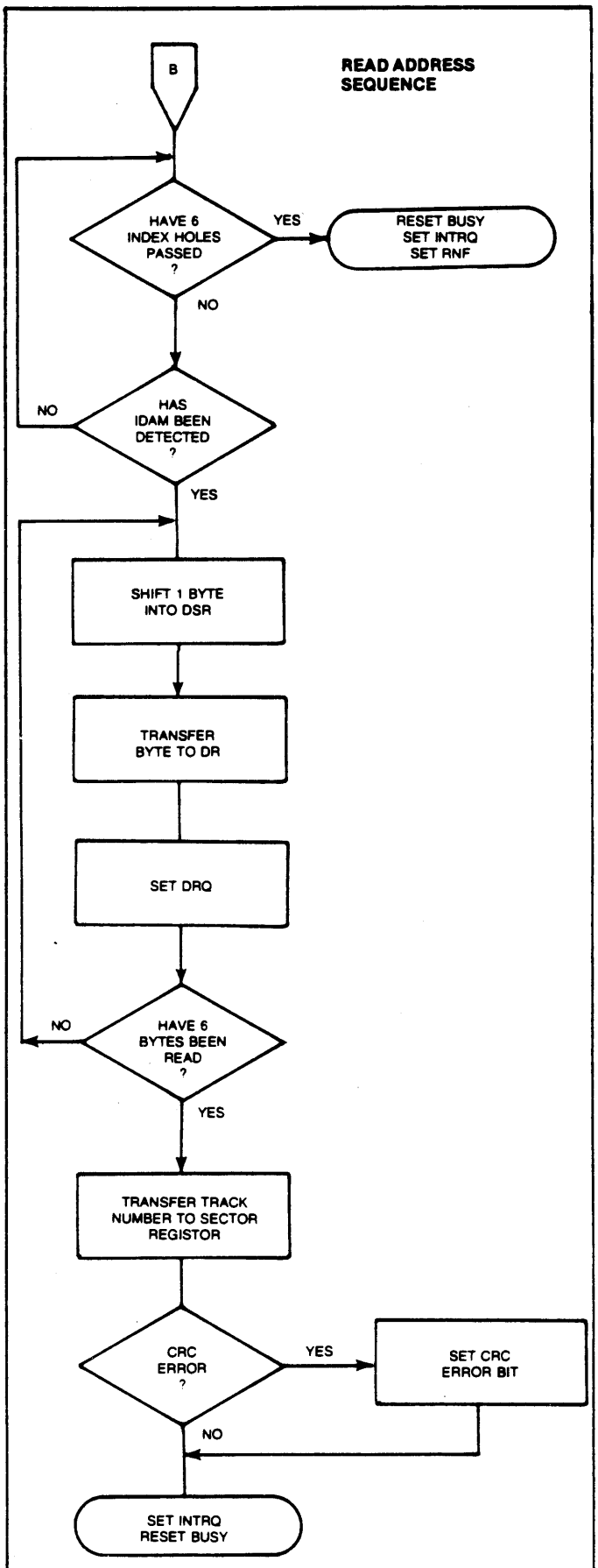
More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT- READY or the next Index Pulse will cause an interrupt condition.

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND

Read Track/Address

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	24 μs	12 μs
Write to Command Reg.	Read Status Bits 1-7	56 μs	28 μs
Write Any Register	Read From Diff. Register	0	0

RECOMMENDED — 128 BYTES/SECTOR

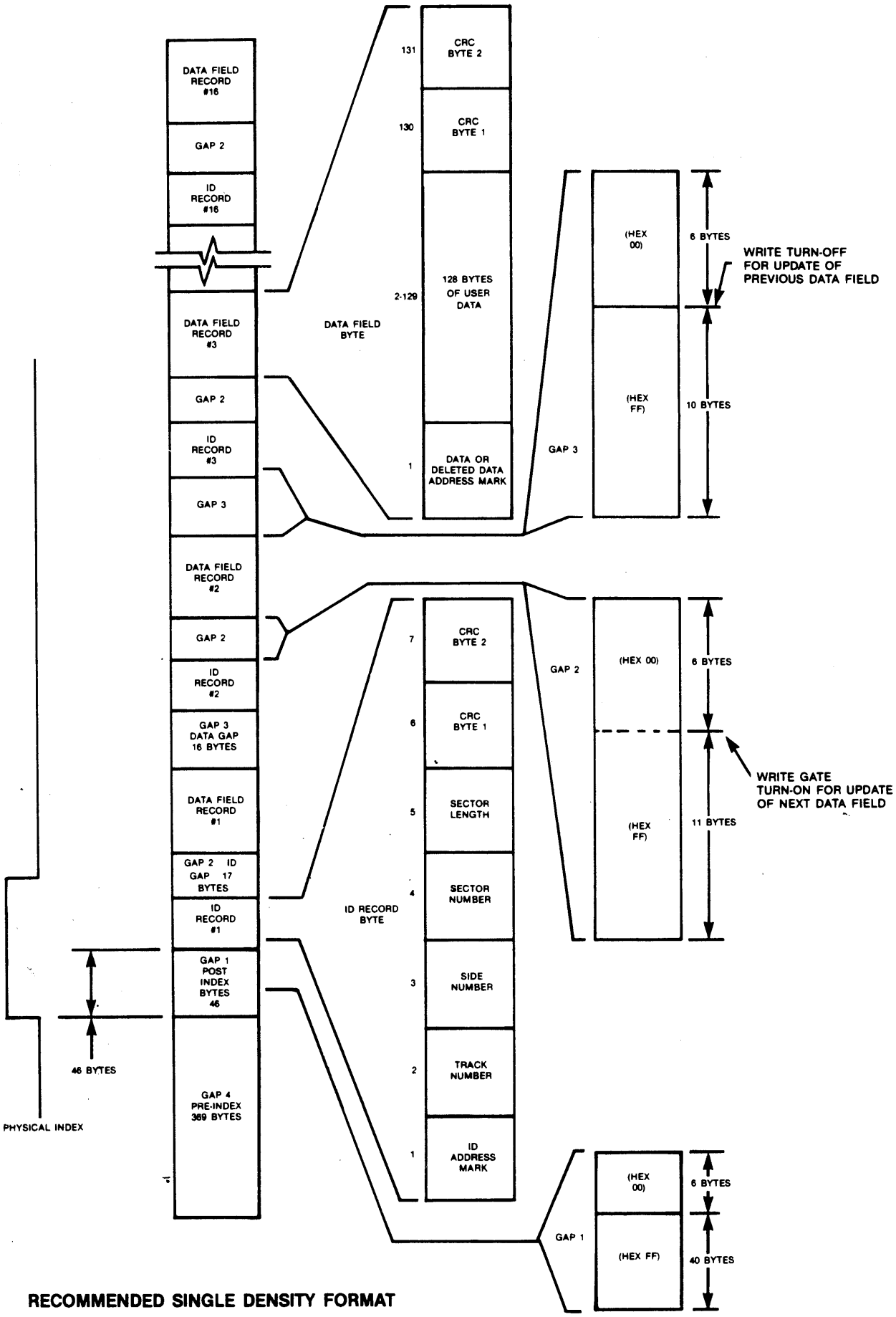
Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF (or 00)[1]
*	6	00
*	1	FE (ID Address Mark)
*	1	Track Number
*	1	Side Number (00 or 01)
*	1	Sector Number (1 thru 1A)
*	1	00 (Sector Length)
*	1	F7 (2 CRC's written)
	11	FF (or 00)[1]
*	6	00
*	1	FB (Data Address Mark)
*	128	Data (IBM uses E5)
*	1	F7 (2 CRC's written)
	10	FF (or 00)[1]
	369**	FF (or 00)[1]

*Write bracketed field 16 times

**Continue writing until FD176X interrupts out. Approx. 324 bytes.

1-Optional '00' on 1765/7 only.



RECOMMENDED SINGLE DENSITY FORMAT

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	60	4E
	12	00
	3	F5 (Writes A1)
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01 (Sector Length)
*	1	F7 (2 CRCs written)
	22	4E
	12	00
	3	F5 (Writes A1)
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRCs written)
	24	4E
	718**	4E

*Write bracketed field 16 times
**Continue writing until FD176X interrupts out. Approx. 668 bytes.

1. NON-STANDARD FORMATS

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.

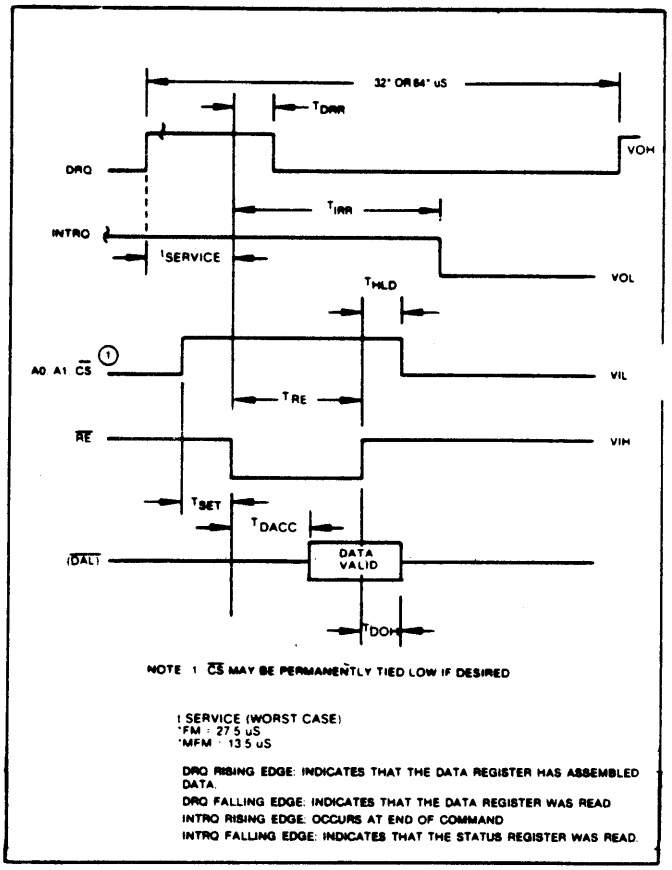
2) Gap 2 cannot be varied from the recommended format.

3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD176X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD176X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



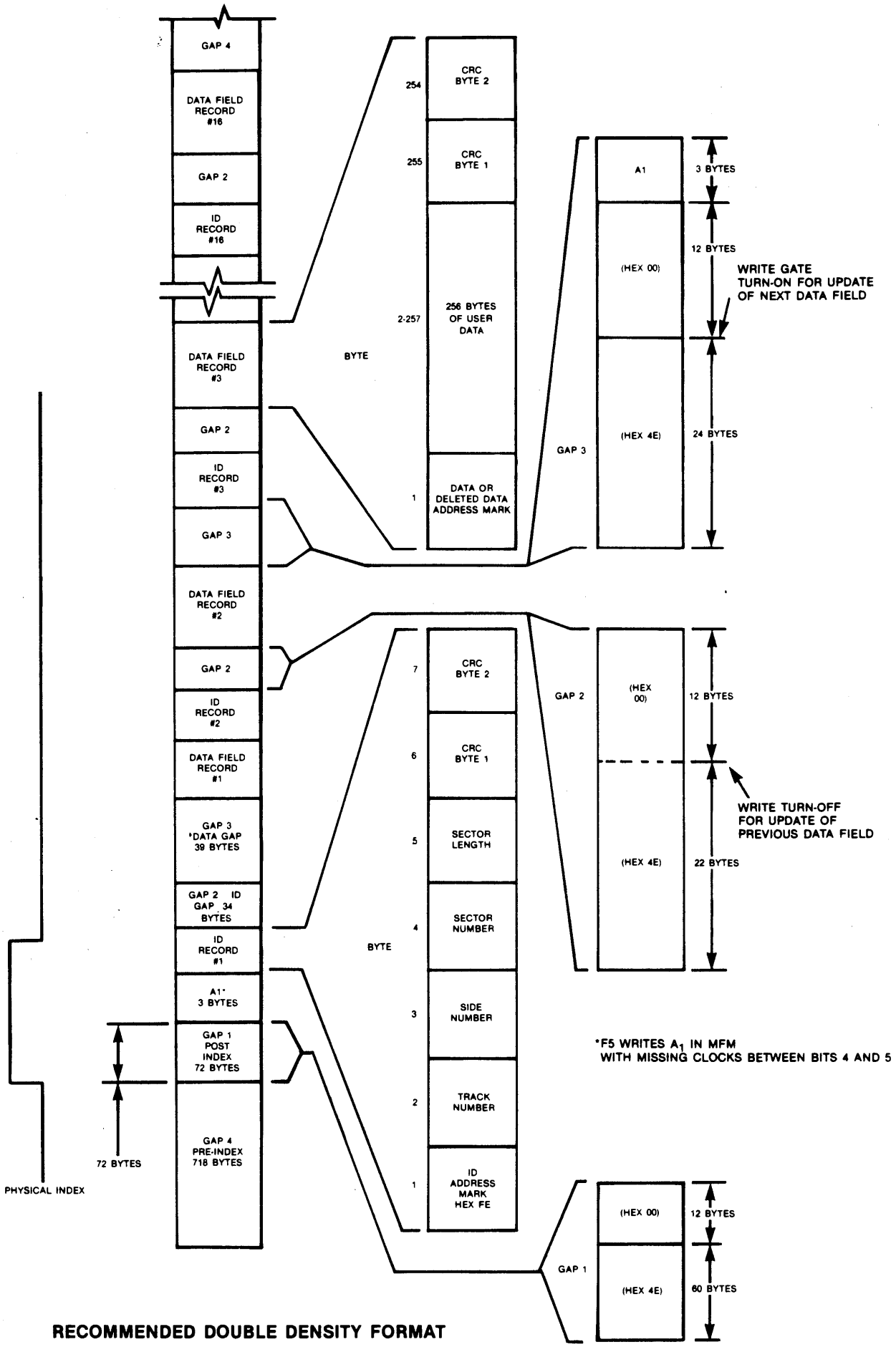
READ ENABLE TIMING

TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

READ ENABLE TIMING (See Note 4, Page 22)

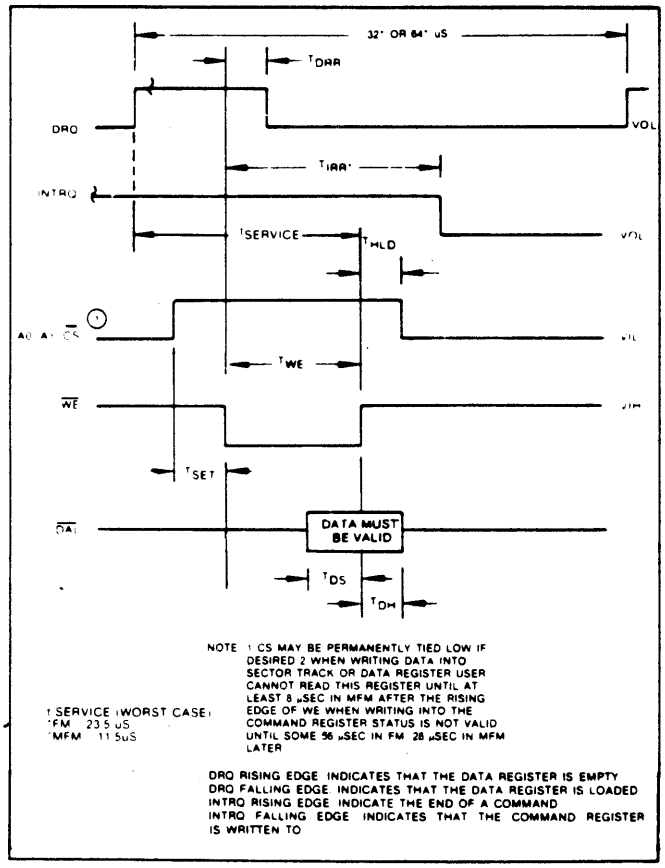
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		1000	6000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 50 pf



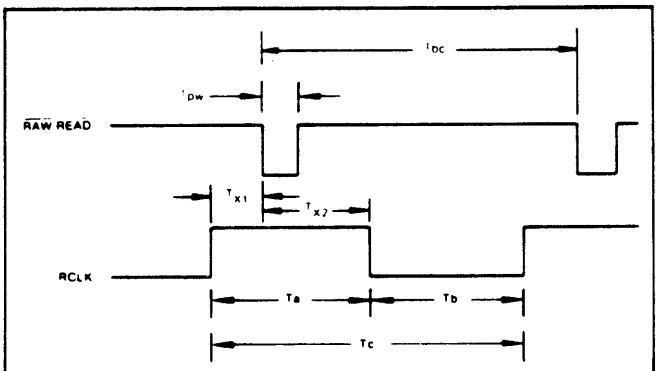
RECOMMENDED DOUBLE DENSITY FORMAT

WRITE ENABLE TIMING (See Note 4, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		1000	6000	nsec	
TDS	Data Access from $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



WRITE ENABLE TIMING



			NOMINAL		
MODE	DDEN	CLK	Ta	Tb	Tc
MFM	0	1 MHz	2 µS	2 µS	4 µS
FM	1	1 MHz	4 µS	4 µS	8 µS

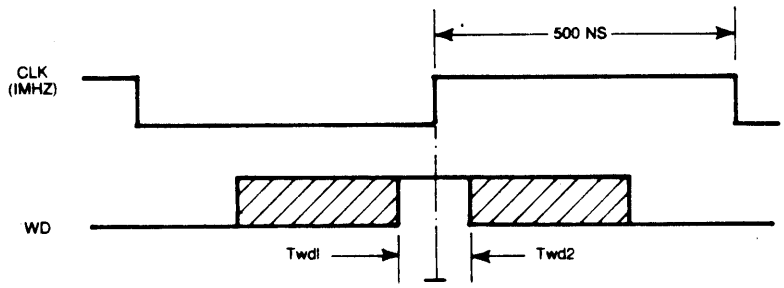
INPUT DATA TIMING (See Note 3, Page 22)

INPUT DATA TIMING (See Note 4, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{Raw\ Read}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{Raw\ Read}$ Cycle Time	3000	4000		nsec	3600 ns @ 70°C
Tc	RCLK Cycle Time	3000	4000		nsec	3600 ns @ 70°C, See Note 2
T_{x1}	RCLK hold to $\overline{Raw\ Read}$	40			nsec	See Note 1
T_{x2}	$\overline{Raw\ Read}$ hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	900	1000	1100	nsec	FM
		300	400	500	nsec	MFM
Twg	Write Gate to Write Data		4		µsec	FM
			2		µsec	MFM
Tbc	Write data cycle Time		4, 6, or 8		µsec	± CLK Error
Ts	Early (Late) to Write Data	250			nsec	MFM
Th	Early (Late) From Write Data	250			nsec	MFM
Twf	Write Gate off from WD		4		µsec	FM
			2		µsec	MFM
Twdl	WD Valid to Clk	100			nsec	
Twd2	WD Valid after CLK	100			nsec	



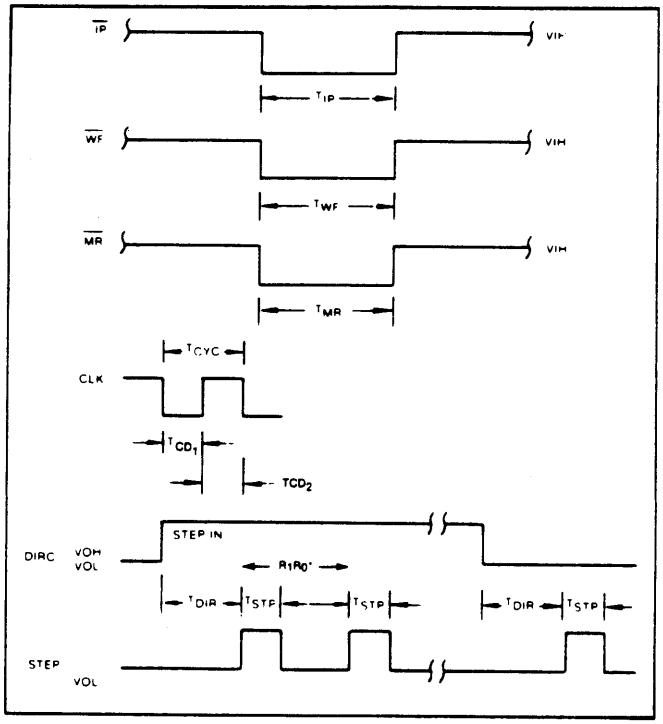
WD MUST HAVE RISING EDGE IN FIRST SHADED AREA AND TRAILING EDGE IN SECOND SHADED AREA.

WRITE DATA/CLOCK RELATIONSHIP IN DOUBLE DENSITY ($\overline{DDEN}$ = 0)

WRITE DATA TIMING

MISCELLANEOUS TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	460	500	20000	nsec	
TCD_2	Clock Duty (high)	400	500	20000	nsec	
TSTP	Step Pulse Output	4 or 8			µsec	
TDIR	Dir Setupt to Step		24		µsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	20			µsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 600 ns for MFM at CLK = 1 MHz and 1200 ns for FM at 1 MHz.
2. tbc should be 4 μs, nominal in MFM and 8 μs nominal in FM.
3. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
4. All timing readings at V_{OL} = .8V & V_{OH} = 2.0V.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

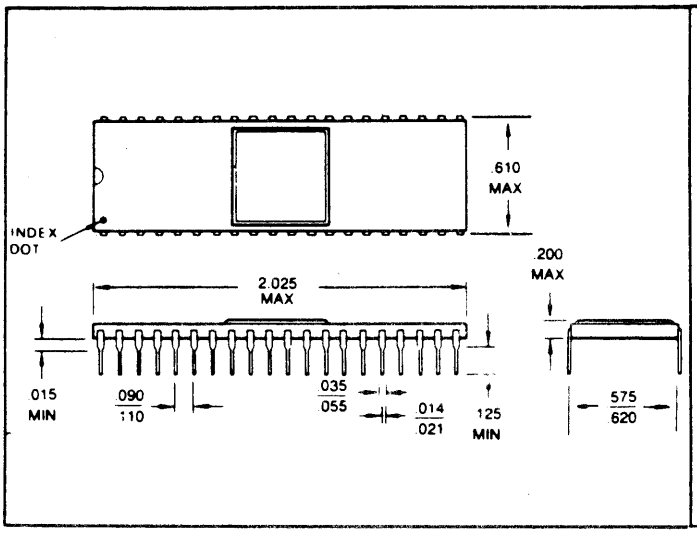
V_{DD} with repect to V_{SS} (ground): + 15 to − 0.3V
Voltage to any input with respect to V_{SS} = + 15 to − 0.3V
I_{CC} = 60 MA (35 MA nominal)
I_{DD} = 15 MA (10 MA nominal)
Dissipation = 0.6 W
C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.
Operating temperature = 0°C to 70°C
Storage temperature = − 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

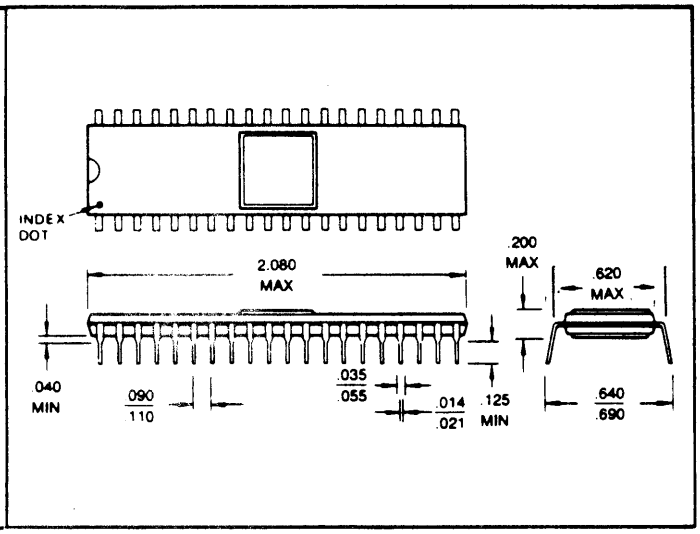
TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{DD}**
I_{OL}	Output Leakage		10	μA	V_{OUT} = V_{DD}
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = − 100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.0 mA
P_D	Power Dissipation		0.6	W	

**Leakage conditions are for input pins without internal pull-up resistors.



FD176XA-02 CERAMIC PACKAGE



FD176XB-02 PLASTIC PACKAGE

NOTES:

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL
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WD2143-03 Four Phase Clock Generator

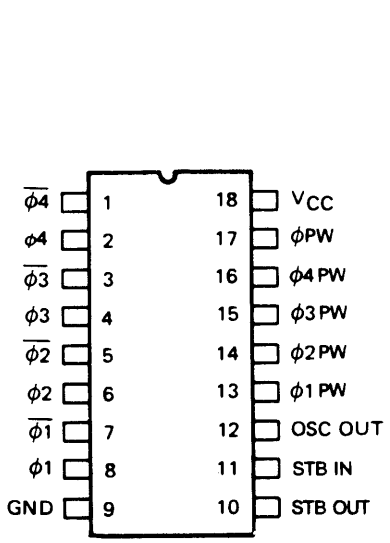
SEPTEMBER, 1981

FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUTS
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate ϕ1PW—ϕ4PW control inputs.



PIN CONNECTIONS

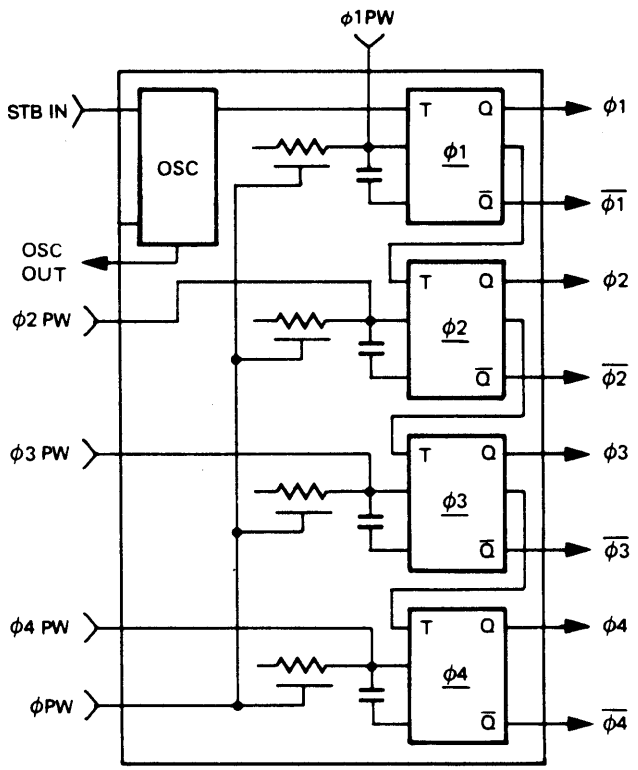


Figure 1 WD2143-03 PIN CONNECTIONS AND BLOCK DIAGRAM

DEVICE OPERATION

Each of the phase outputs can be controlled individually by typing an external resistor from ϕ1PW-ϕ4PW to a +5V supply. When it is desired to have ϕ1 through ϕ4 outputs the same width, the ϕ1PW-ϕ4PW inputs should be left open and an external resistor tied from the ϕPW (Pin 17) input to +12V.

STROBE IN (pin 11) is driven by a TTL square wave with STROBE OUT (pin 10) left open. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{\phi 1}$—$\overline{\phi 4}$	Four phase clock outputs. These outputs are inverted (active low).
2, 4, 6, 8	$\phi 1$-$\phi 4$	Four Phase clock outputs. These outputs are true (active high).
9	GND	Ground
10	STB OUT	This pin is left unconnected.
11	STB IN	Input signal to initiate four-phase clock outputs.
12	N.C.	No connection
13-16	ϕ1PW-ϕ4PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ϕPW is used.
17	ϕPW	External resistor input to control all phase outputs to the same pulse widths.
18	V_{cc}	+5V ± 5% power supply input

Table 1 PIN DESCRIPTIONS

TYPICAL APPLICATIONS

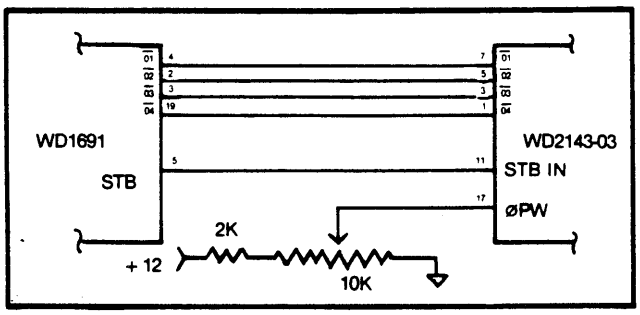


Figure 2 WRITE PRECOMP OPERATION WITH F.S.L. WD1691

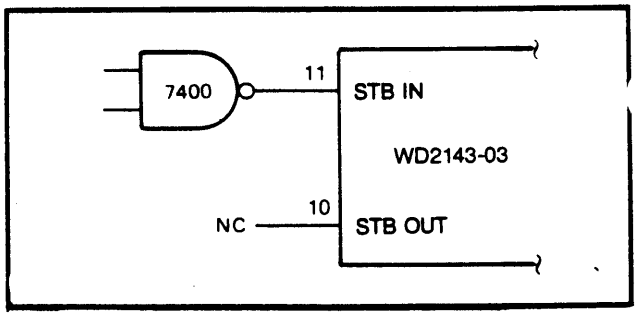


Figure 3 TTL SQUARE WAVE OPERATION

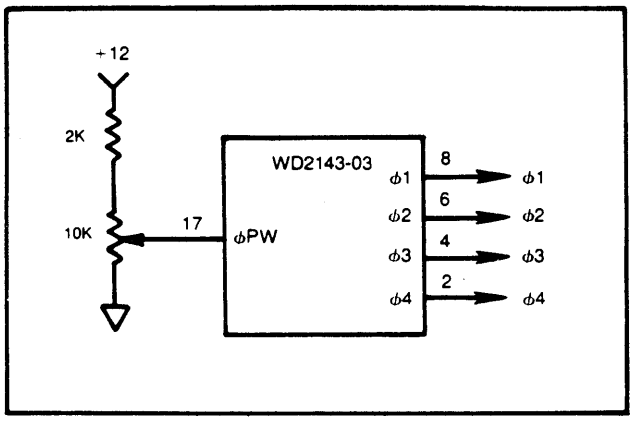


Figure 4 EQUAL PULSE WIDTH OUTPUTS

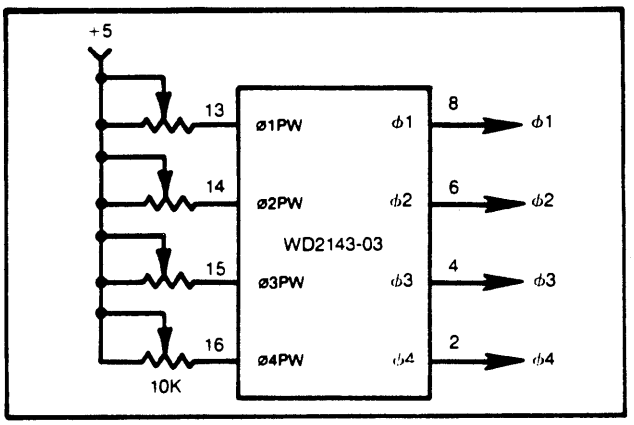


Figure 5 INDIVIDUAL PULSE WIDTH OUTPUTS

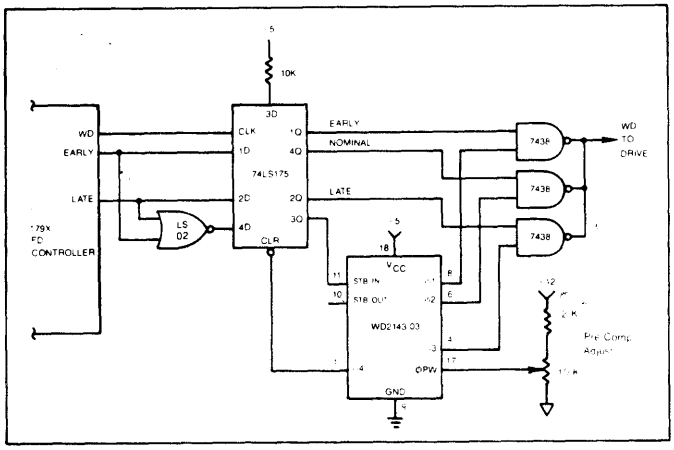


Figure 6 WRITE PRECOMP FOR FLOPPY DISK

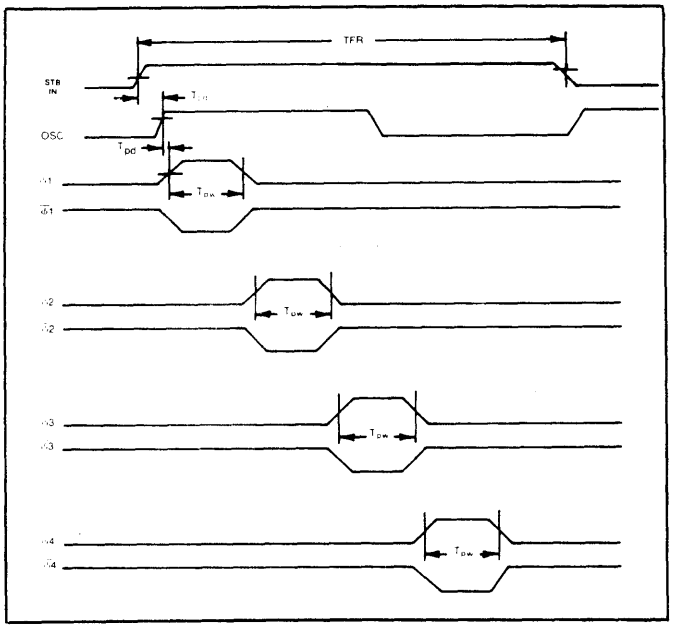


Figure 7 WD2143-03 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings		
Operating Temperature		0° to +70° C
Voltage on any pin with respect to Ground*		−0.5 to +7V
Power Dissipation		1 Watt
Storage Temperature	plastic	−55° to +125° C
	ceramic	−65° to +150°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

*Pin 17 = −0.5V to +12V. Increasing voltage on Pin 17 will decrease T_{pw}.

DC ELECTRICAL CHARACTERISTICS

V_{cc} = 5V ±5%, GND = OV, T_A = 0° to 70°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{ol}	TTL low level output		0.4	V	I_{ol} = 1.6 ma.
V_{oh}	TTL high level output	2.4		V	I_{oh} = −100 ua.
V_{il}	STB in low voltage		0.8	V	
V_{ih}	STB in high voltage	2.4		V	
I_{cc}	Supply Current		80	ma	All outputs open

Table 2 DC ELECTRICAL CHARACTERISTICS

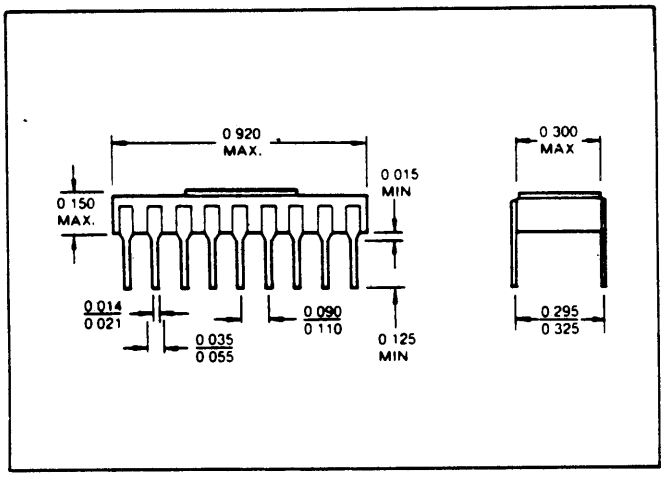
SWITCHING CHARACTERISTICS

V_{CC} = 5V ± 5%, GND = 0V T_A = 0° to 70° C

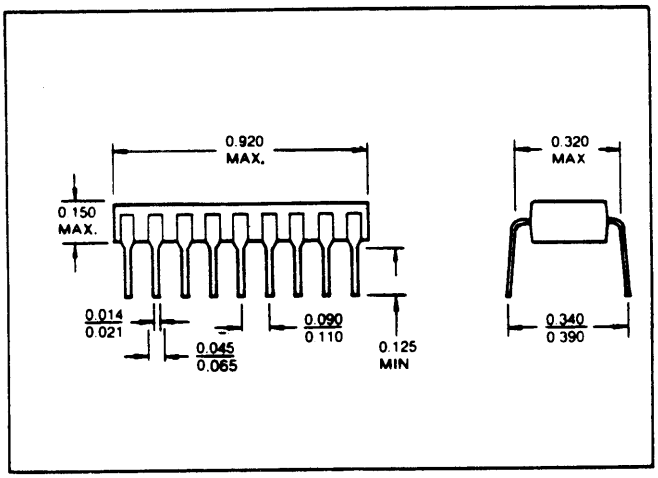
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{cd}	STB IN to OSC out (↑)		70	NS	
T_{pd}	STB OUT to ϕ1		70	NS	
T_{pw}	Pulse Width (any output)	100	300	NS	CL = 30pf
T_{pr}	Rise Time (any output)		30	NS	CL = 30 pf
T_{pf}	Fall Time (any output)		25	NS	CL = 30 pf
TFR	STROBE Frequency		2.5	MHz	combined Tpw = 400 NS.
T_{dpw}	Pulse Width Differential		10	%	100–300 NS.

Table 3 SWITCHING CHARACTERISTICS

NOTE: T_{pw} measured at 50% V_{OH} Point; V_{OL} = 0.8V, V_{OH} = 2.0V.



WD2143L-03 CERAMIC PACKAGE



WD2143M-03 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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SHUGART 801R CONNECTIONS

1. Single Drive

A. Connection of input signals as per diagram no. 1

B. Jumpers as per diagram no. 1.

C. Operation - In this configuration the drive will be selected when a logic Ø is applied to pin J1-26. The IN USE LED (this is the light in the disk door latch) will come on and stay on whenever the drive is selected. The head load solenoid will be activated when a logic Ø is applied to J1-18 and the disk access door is closed. The stepper motor will be enabled all the time power is applied to disk drive.

2. Two Drives.

A. Connection of input signals are the same as for single drive see diagram no. 2

B. Jumpers are placed per diagram no. 2. If jumpers for T1, T3, T4, T5, and T6 are installed on first drive they should not be installed on second drive. An ideal situation would be to have T1 and T3 thru T6 jumpered only on the last drive on the input signal cable. The connection from pin J1-26 to T2 must be cut as shown on diagram no. 2.

2. TWO DRIVES (cont.)

C. OPERATION - BOTH DRIVES WILL PERFORM AS INDICATED FOR SINGLE DRIVE.

3. MORE THAN 2 DRIVES.

A. CONNECTION OF INPUT SIGNALS AS SHOW IN DIAGRAMS 1 AND 2.

B. JUMPERS should be PLACED AS DISCUSSED IN SECTION 3 OF TWO DRIVES. ONLY THE DRIVE select JUMPER WILL be DIFFERENT. FOR DRIVE 3 select, A JUMPER IS PLACED AT PIN J1-30 AND FOR DRIVE 4 select, A JUMPER IS PLACED AT J1-32. The HARD WIRED JUMPER AT J1-26 MUST be CUT. See DIAGRAMS 3 AND 4.

C. OPERATION OF DRIVES WILL BE SAME AS DISCUSSED FOR A SINGLE DRIVE AS FAR AS SIGNALS DRIVE select, HEAD LOAD, AND IN USE LED AND STEPPER MOTOR ARE CONCERNED.

4. OPTIONAL DRIVE OPERATION.

A. This option can not be used in drive position one in most cases due to the way boot software is written. It will work fine in all other drive positions.

B. This option will allow a head load and a stepper motor enable only when the drive is selected. The advantages are a cooler running stepper motor and less useage of head load solonoid.

C. See diagram no. 5 on how to set up this option.

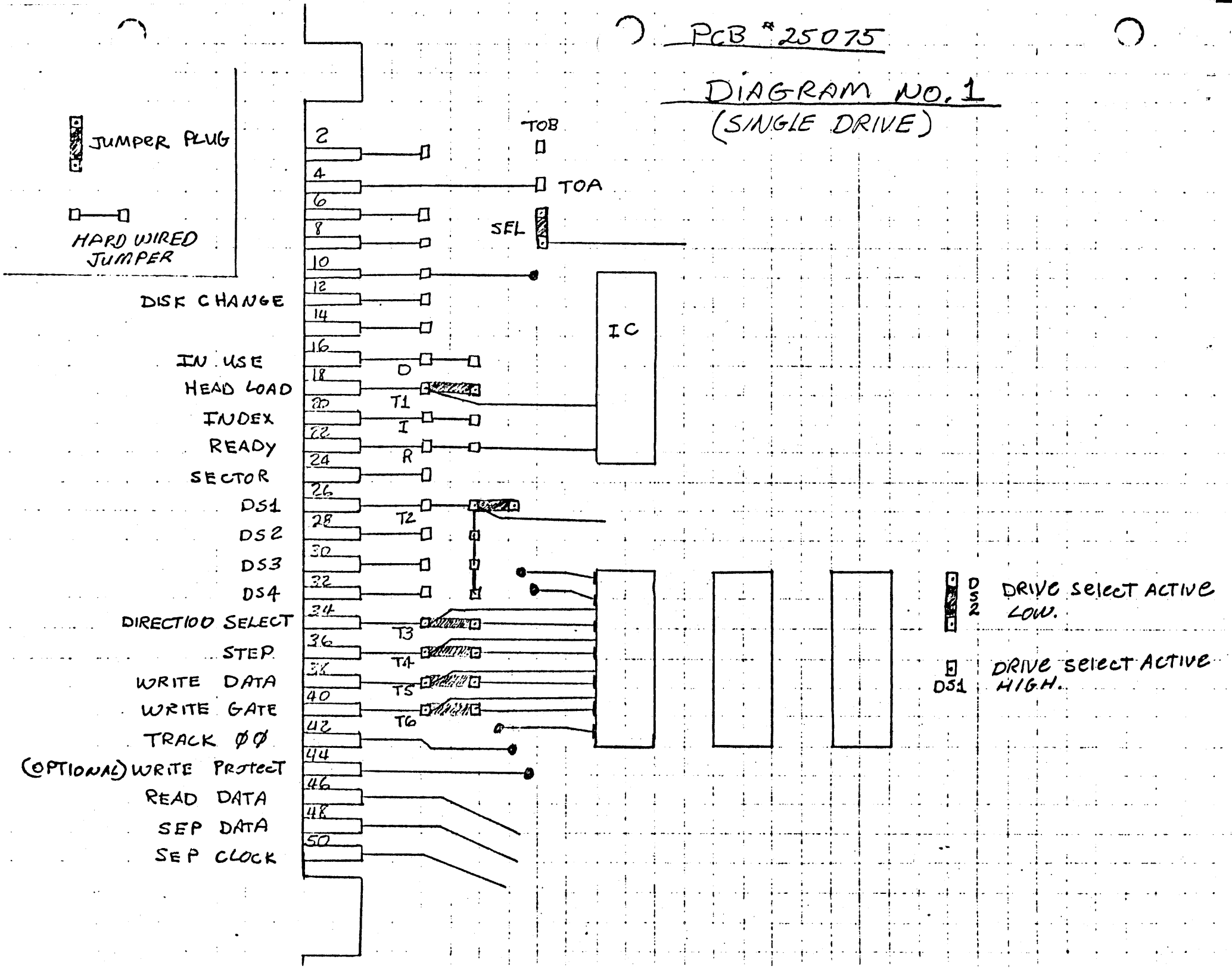
5. OPTIONAL DRIVE OPERATION FOR FIRST DRIVE (Boot Drive)

A This option will allow the head load solonoid to be activated only when drive is selected. The stepper motor will be enabled whenever a step signal and track 00 signal is applied. This will allow the stepper motor to run much cooler than if it were enabled all the time.

B See diagram no. 6 for set up.

PCB #25075

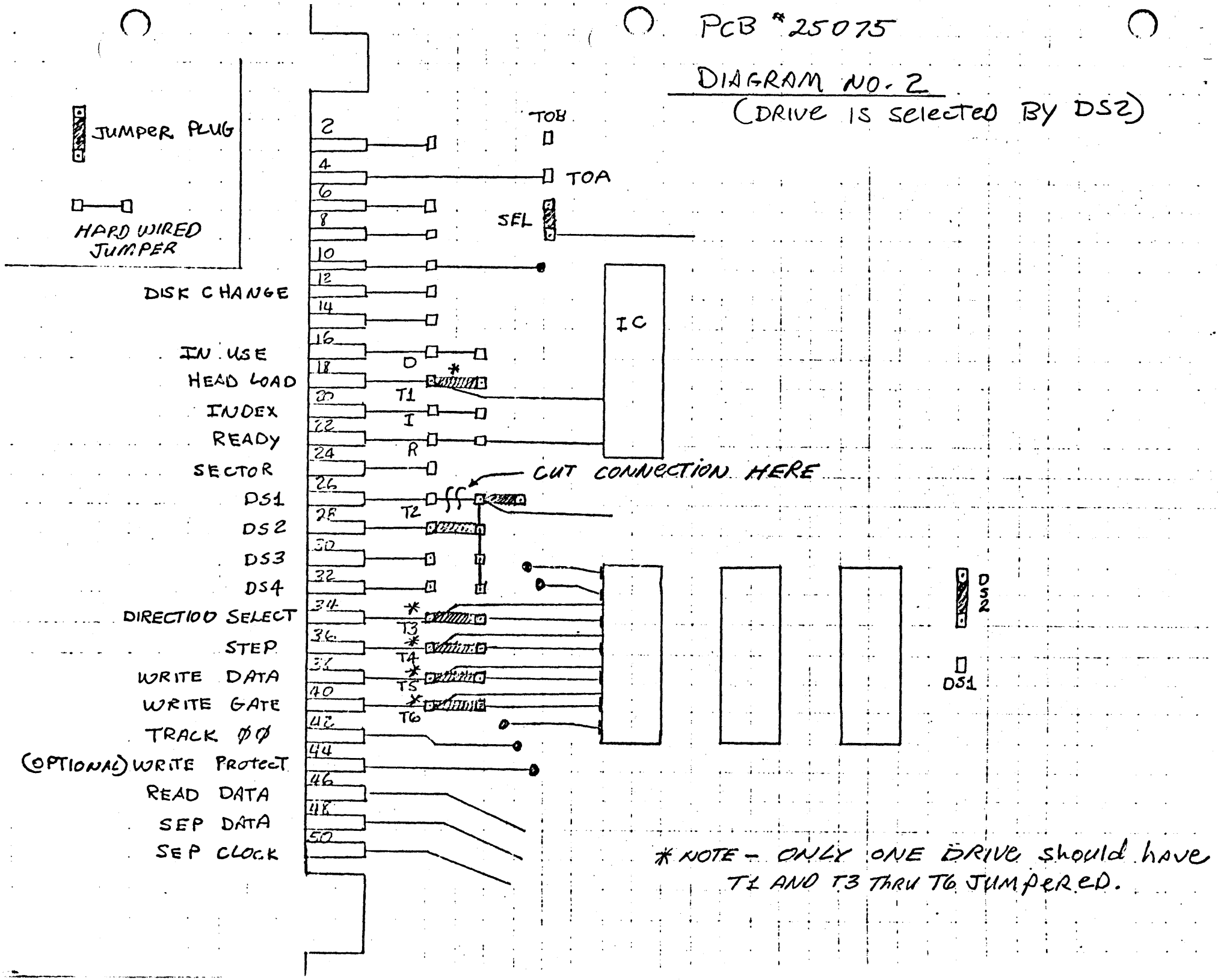
DIAGRAM NO. 1
(SINGLE DRIVE)



PCB #25075

DIAGRAM NO. 2

(DRIVE IS SELECTED BY DS2)



*NOTE - ONLY ONE DRIVE should have T1 AND T3 THRU T6 JUMPERED.

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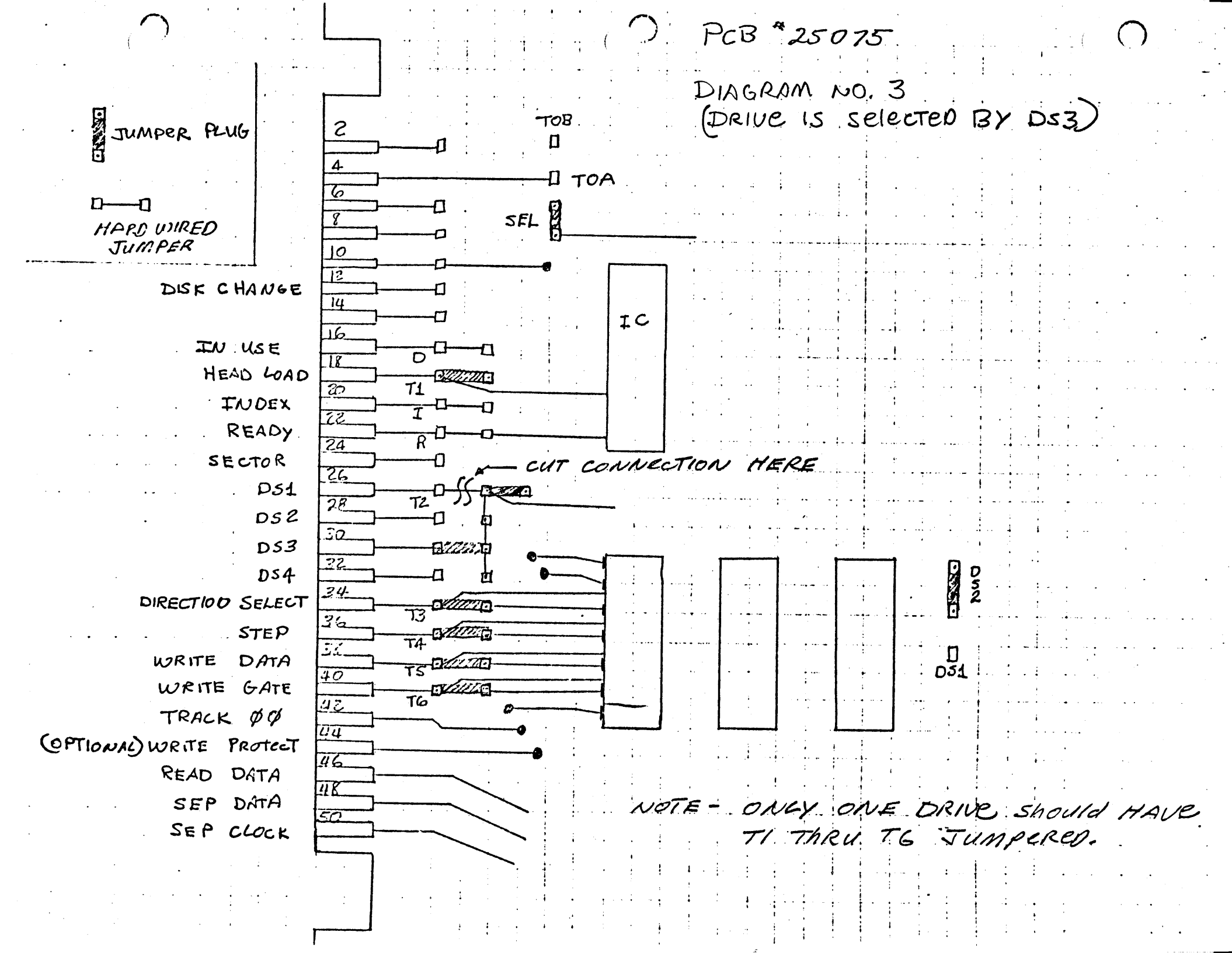
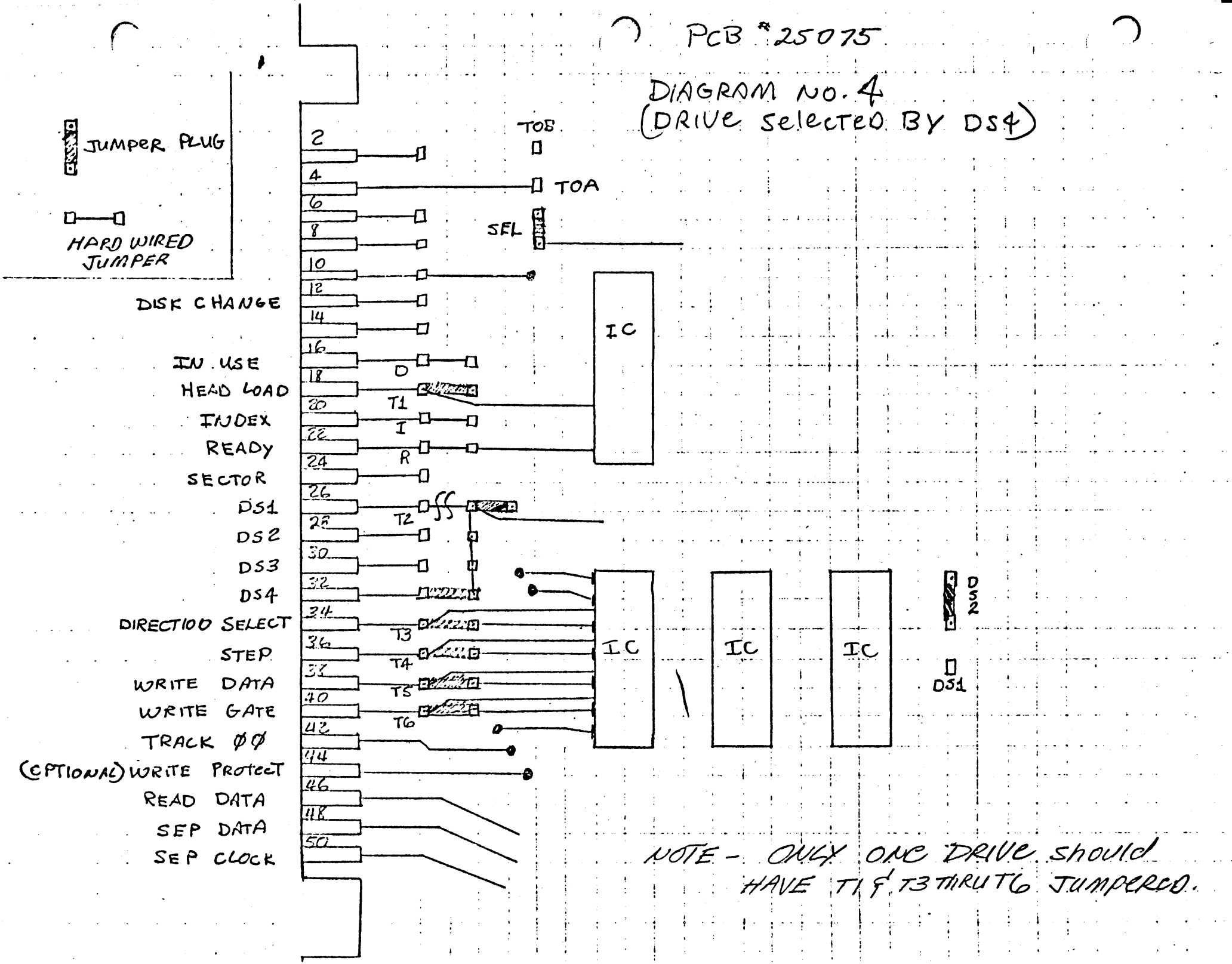
DIAGRAM NO. 3
(DRIVE IS SELECTED BY DS3)



NOTE - ONLY ONE DRIVE SHOULD HAVE T1 THRU T6 JUMPERED.

PCB #25075

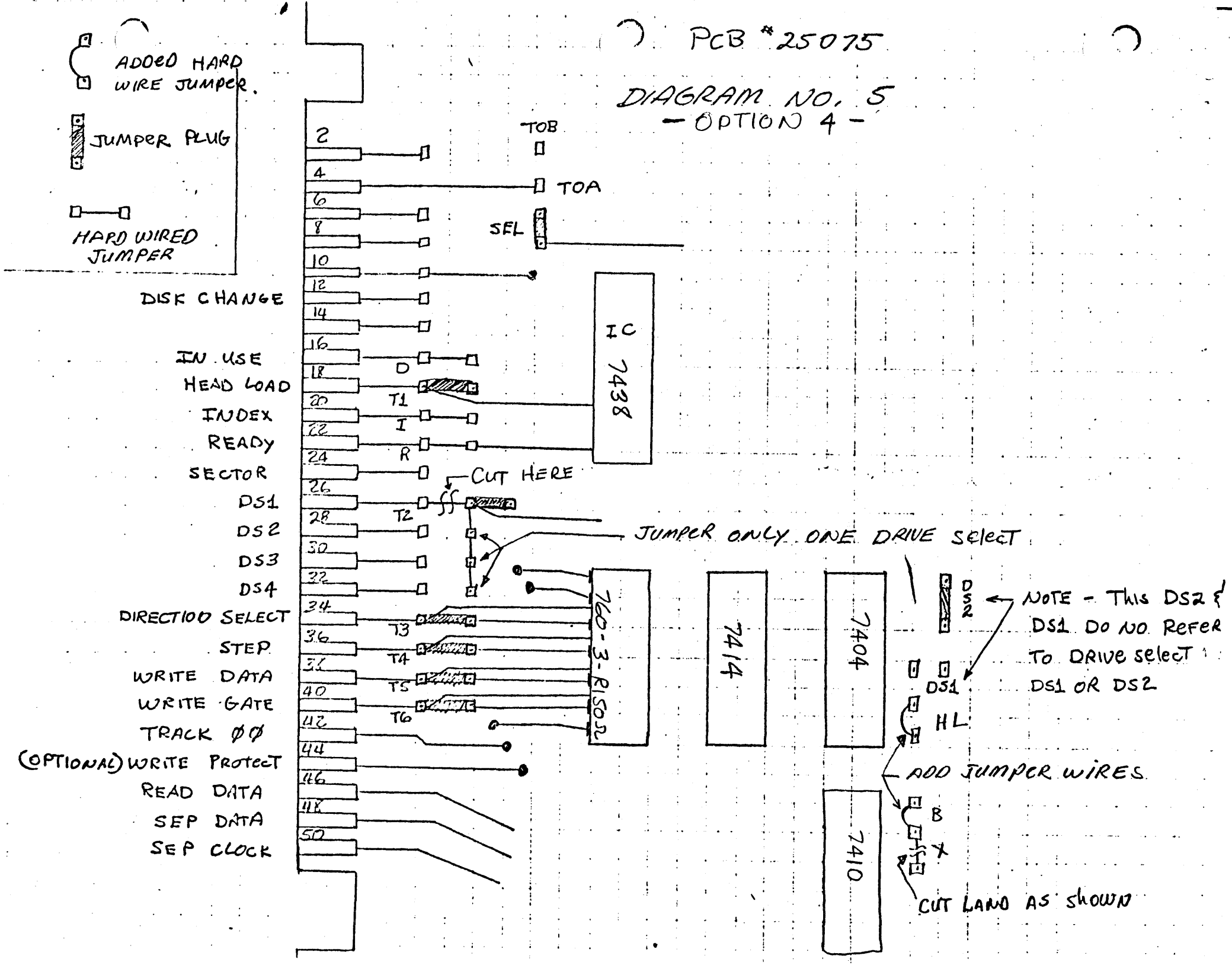
DIAGRAM NO. 4
(DRIVE SELECTED BY DS4)



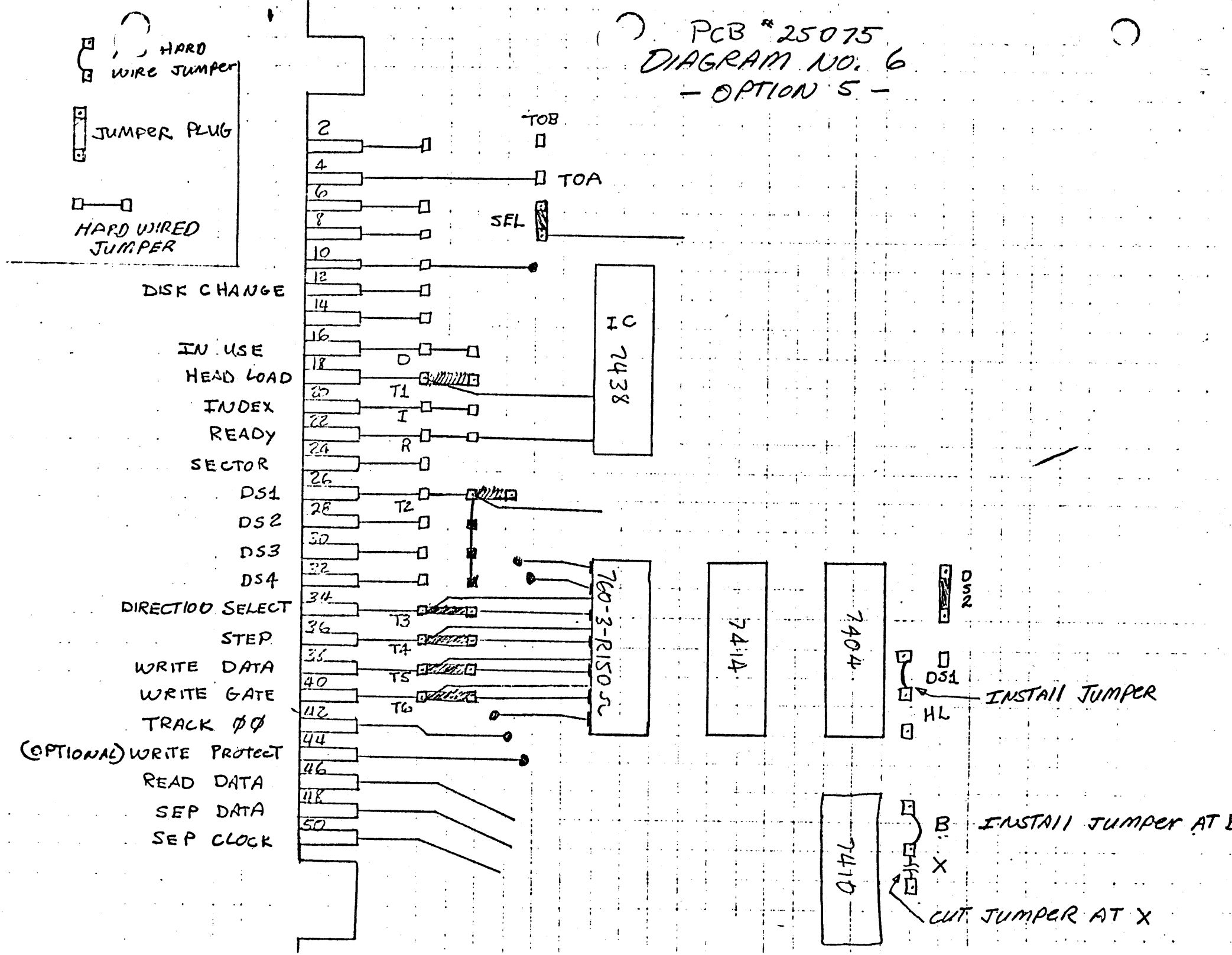
NOTE - ONLY ONE DRIVE should HAVE T1 & T3 THRU T6 JUMPERED.

PCB #25075

DIAGRAM NO. 5
— OPTION 4 —

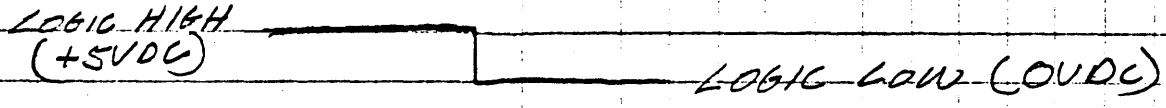


PCB #25075
DIAGRAM NO. 6
— OPTION 5 —



SCHEMATIC Notes:

1. A MINUS SIGN OR DASH - IN FRONT OF SIGNAL NAME IMPLIES IT IS ACTIVE WHEN GOING FROM A LOGIC HIGH TO A LOGIC LOW.



2. IF THE DRIVE select inputs AT PINS J1-26 THRU J1-32 ARE ACTIVE GOING LOW FROM DISK CONTROLLER THAN USE DS2 SHORTIN PLUG (See AREA ABOVE TP11 ON SCHEMATIC).

IF DRIVE SELECT SIGNALS ARE ACTIVE GOING HIGH FROM CONTROLLER THAN USE DS1 SHORTING PLUG.

3. WITH The FOLLOWING SHORTING PLUGS INSTALLED The DRIVE WILL BE SET UP To WORK WITH ANY CONTROLLER FOLLOWING ANSI STANDARDS FOR DISK DRIVE To CONTROLLER SIGNALS AND CONTROLLER TO DISK DRIVE SIGNALS.

PLACE SHORTING PLUGS AT - T1
T2
T3
T4
T5
T6
SEL
DS2

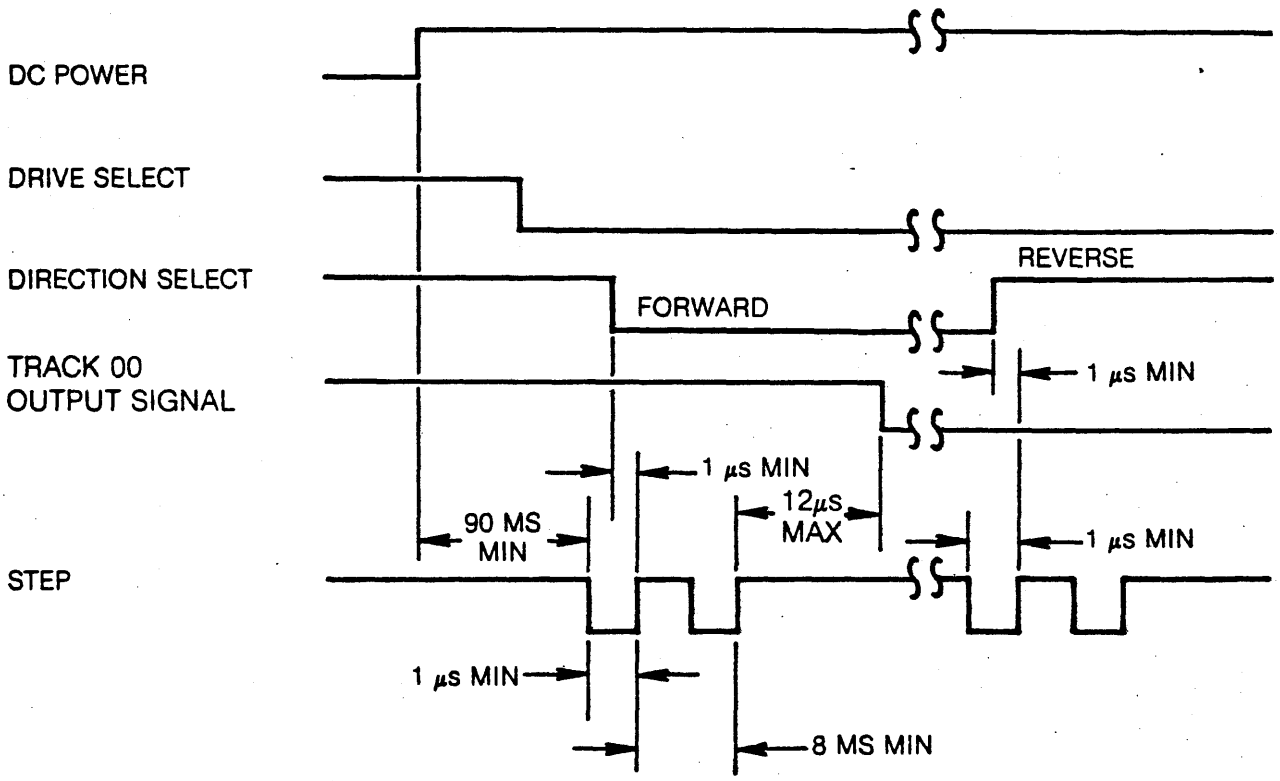
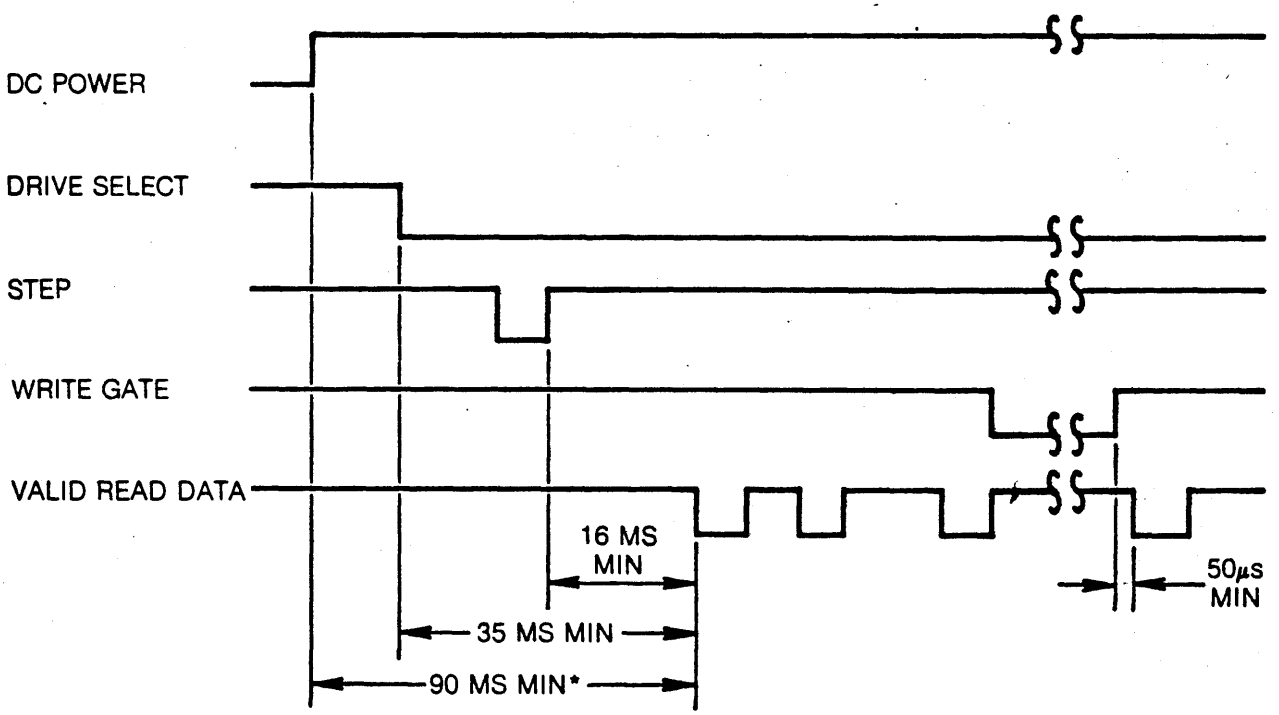
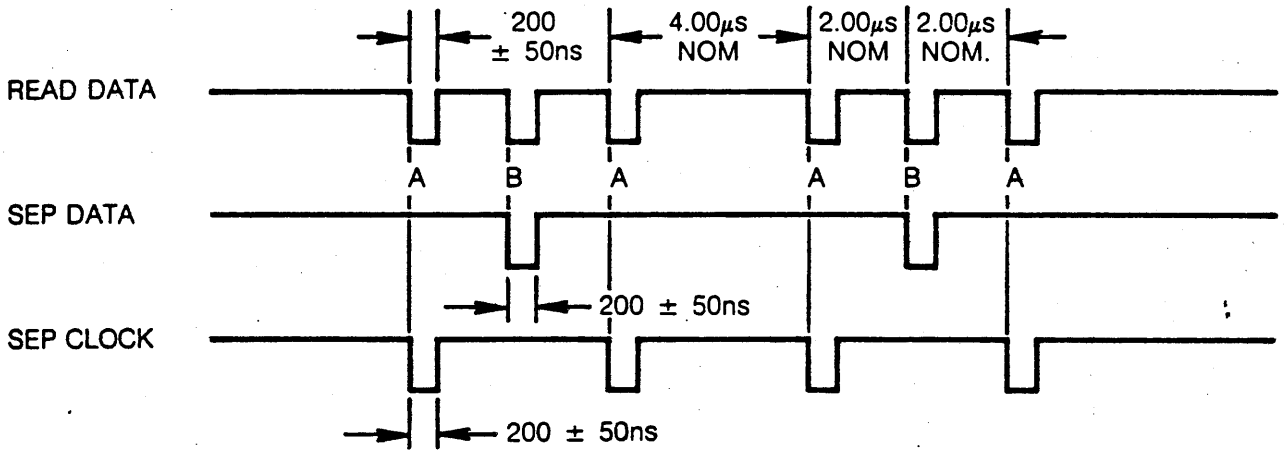


Figure 3. Track Access Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

Figure 4. Read Initiate Timing



A = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 200 ns FROM ITS NOMINAL POSITION.

Figure 5. Read Signal Timing

3.5 Write Operation

Writing data to the SA800/801 is accomplished by:

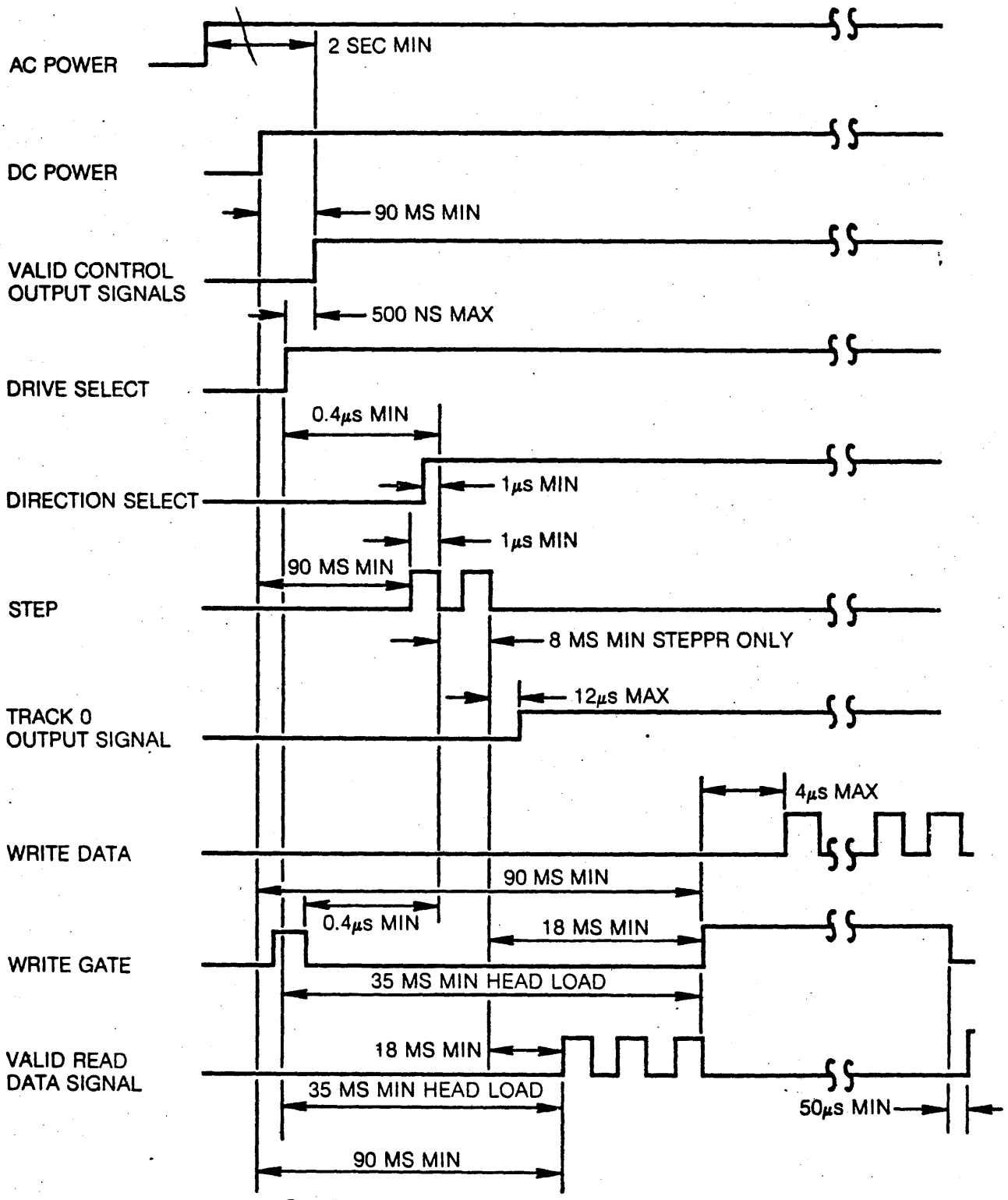
a. Activating the Drive Select line.
b. Activating the Write Gate line.
c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in Figure 7.

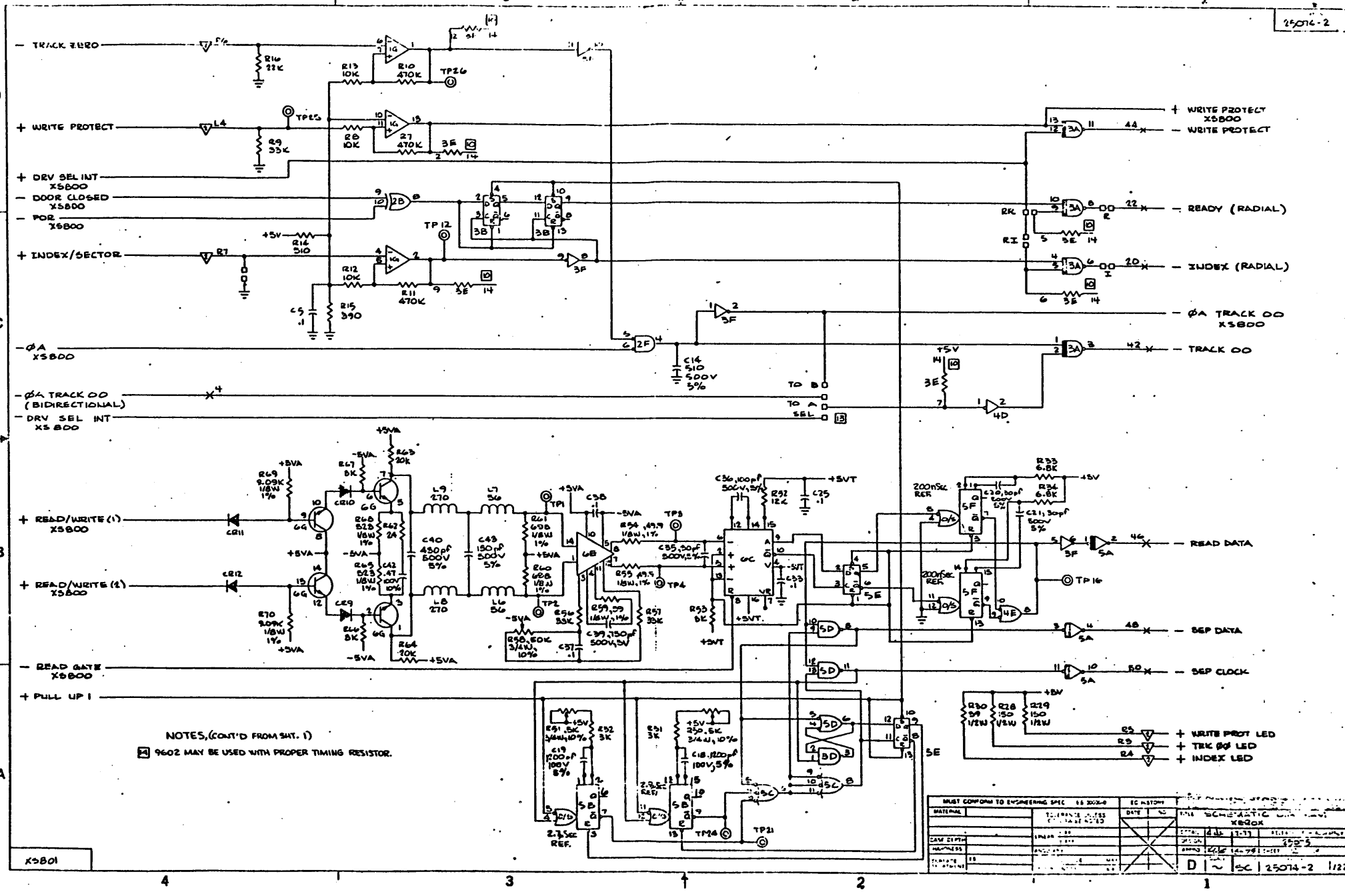
3.6 Sequence of Events

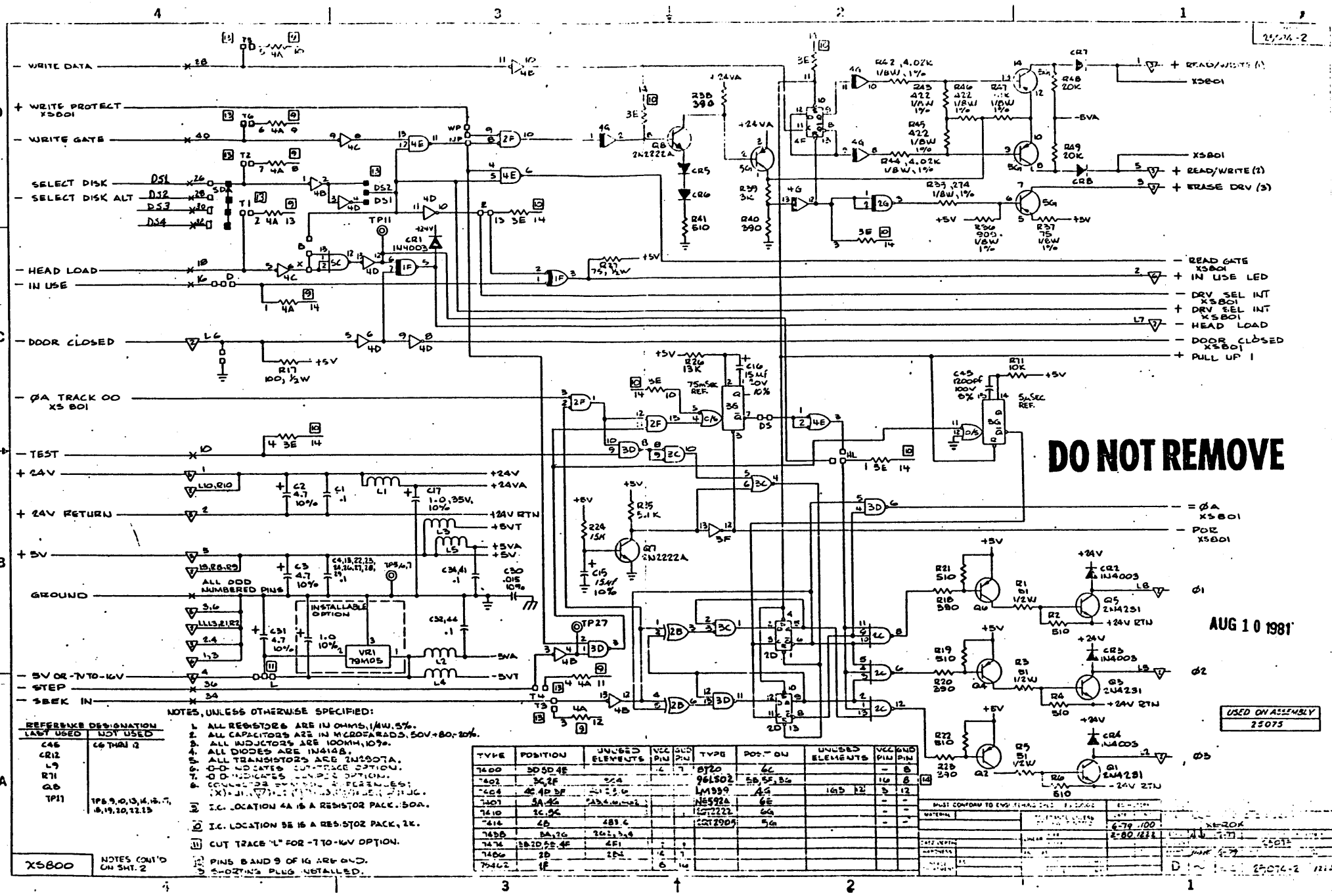
The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.



NOTE 1: 35ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, than and 8ms minimum delay must be introduced to allow for stepper settling.

General Control and Data Timing Requirements


TRACK ZERO
WRITE PROTECT
DRV SEL INT X5800
DOOR CLOSED X5800
POR X5800
INDEX/SECTOR
-ØA X5800
-ØA TRACK 00 (BIDIRECTIONAL)
DRV SEL INT X5800
READ/WRITE (1) X5800
READ/WRITE (2) X5800
READ GATE X5800
PULL UP 1
+ WRITE PROTECT X5800
- WRITE PROTECT
- READY (RADIAL)
- INDEX (RADIAL)
- ØA TRACK 00 X5800
- TRACK 00
TO B SEL
TO A SEL
- READ DATA
- SEP DATA
- SEP CLOCK
+ WRITE PROT LED
+ TRK Ø0 LED
+ INDEX LED
NOTES,(CONT'D FROM SHT. 1)
[4] 9602 MAY BE USED WITH PROPER TIMING RESISTOR.
X5801
25074-2


DO NOT REMOVE
AUG 10 1981
WRITE DATA
WRITE PROTECT
WRITE GATE
SELECT DISK
SELECT DISK ALT
HEAD LOAD
IN USE
DOOR CLOSED
ØA TRACK 00
TEST
+24V
+24V RETURN
+5V
GROUND
-5V OR -7 TO -16V
STEP
SEEK IN
READ/WRITE (1)
READ/WRITE (2)
ERASE DRV (3)
READ GATE
+ IN USE LED
DRV SEL INT
HEAD LOAD
DOOR CLOSED
+ PULL UP 1
=ØA
POR
Ø1
Ø2
Ø3
INSTALLABLE OPTION
ALL ODD NUMBERED PINS
NOTES, UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V +80,-20%.
3. ALL INDUCTORS ARE 100MH, 10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2907A.
6. O-O INDICATES CUT TRACE OPTION.
7. O-O INDICATES JUMPER OPTION.
8. CONNECTOR SYMBOLS & REFERENCES: (X)-J1, (Y)-P1, (Z)-P2.
9. I.C. LOCATION 4A IS A RESISTOR PACK, 50A.
10. I.C. LOCATION 3E IS A RESISTOR PACK, 2K.
11. CUT TRACE "L" FOR -7 TO -16V OPTION.
12. PINS 8 AND 9 OF IG ARE GND.
13. SHORTING PLUG INSTALLED.
REFERENCE DESIGNATION
LAST USED: C46, CR12, L9, R71, Q8, TP21
NOT USED: C6 THRU 12; TP5,9,10,13,14,15,17,18,19,20,22,23
XS800
NOTES CONT'D ON SHT. 2
USED ON ASSEMBLY 25075
XEROX
25074-2

25074-2

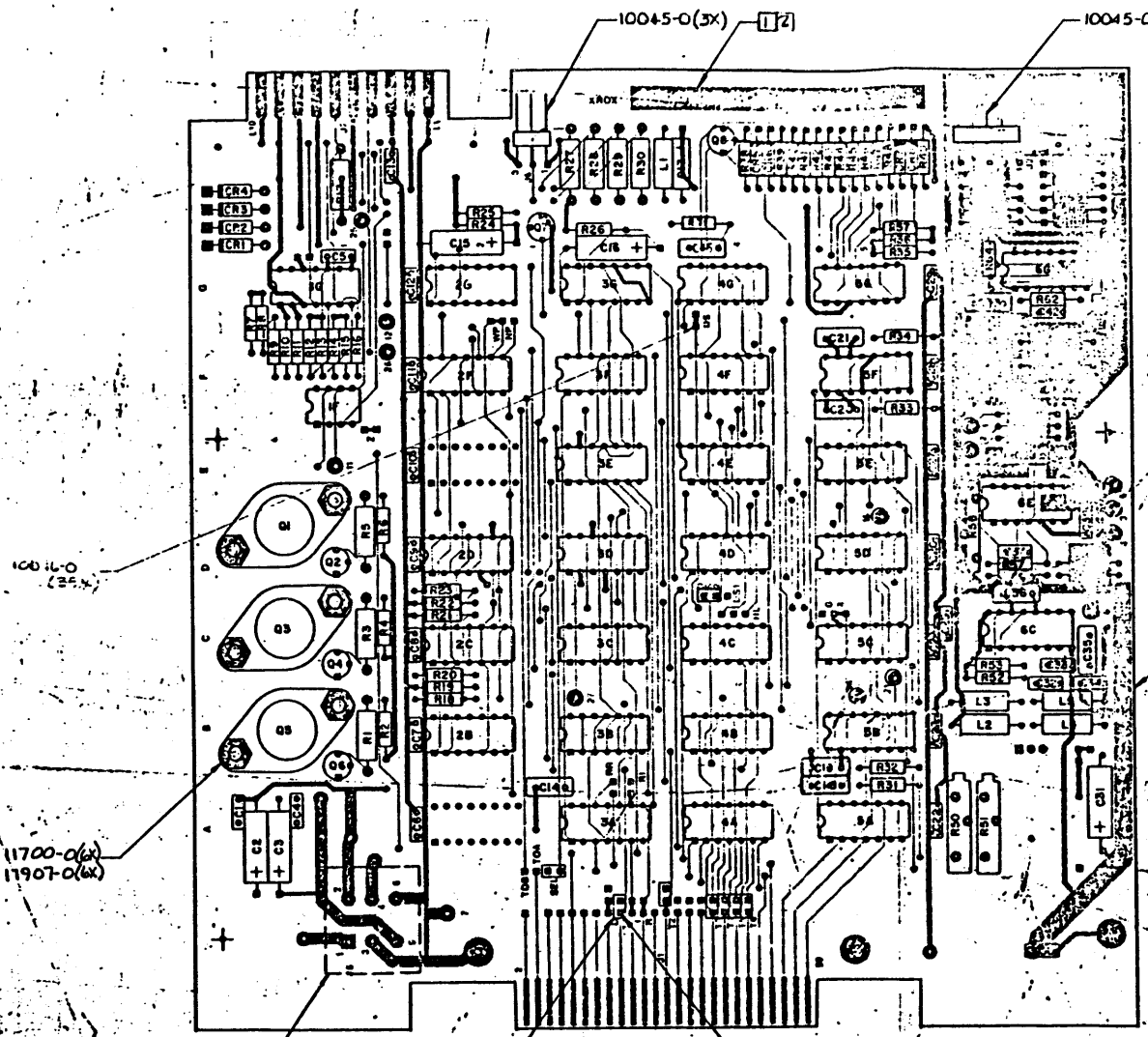


TABLE 1

ASSEMBLY CODE	ASSEMBLY PART NUMBER	ASSEMBLY EC	ASSEMBLY KIT EC LEVEL 25076-0			
0A	25075-2	1288	1288			

SUPPORT DOCUMENTS

CODE	PART NUMBER	EC
SC	25074-2	1222
TI		
P.A	25074-2	1222

AUG 10 1981

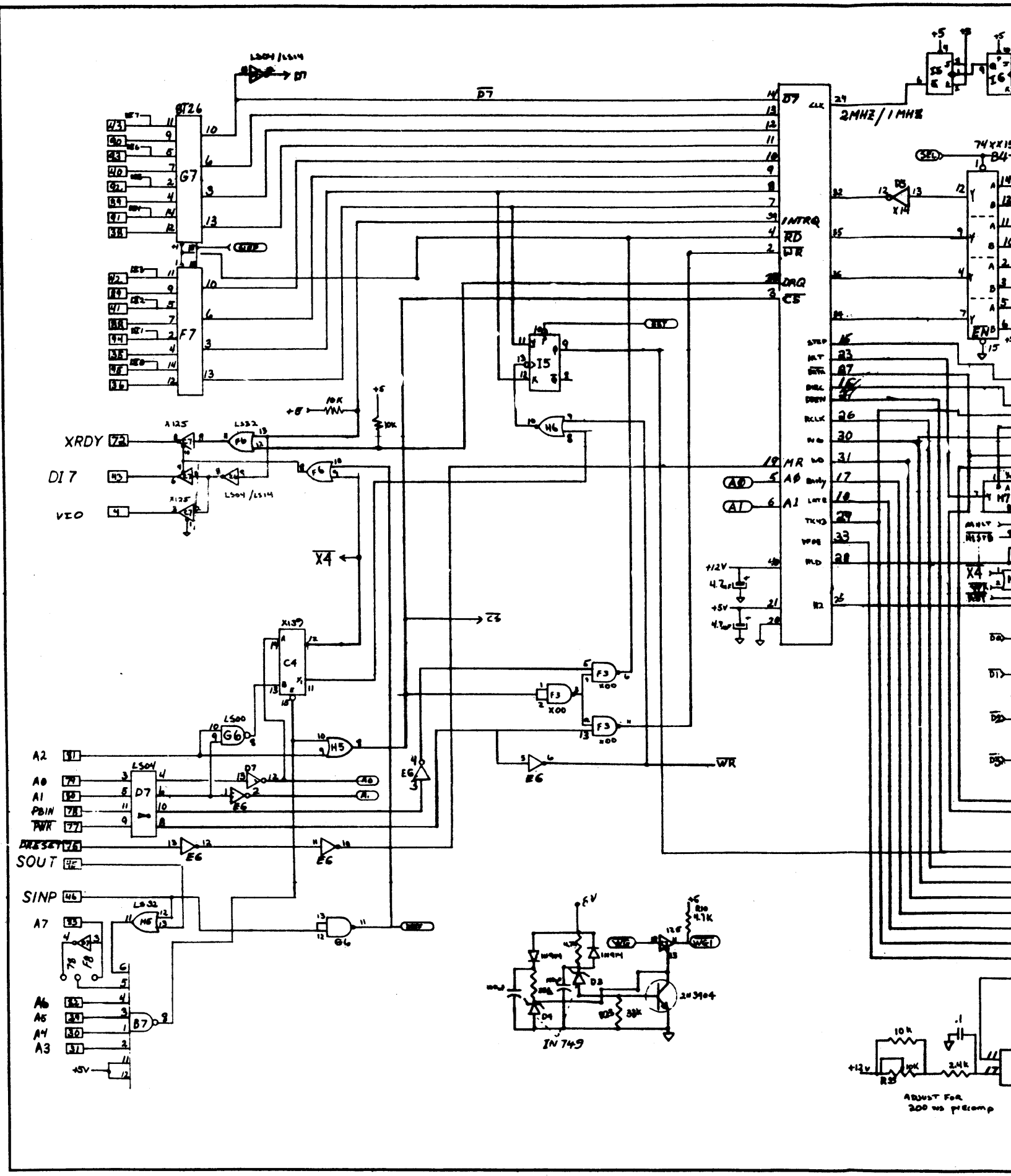
DO NOT REMOVE

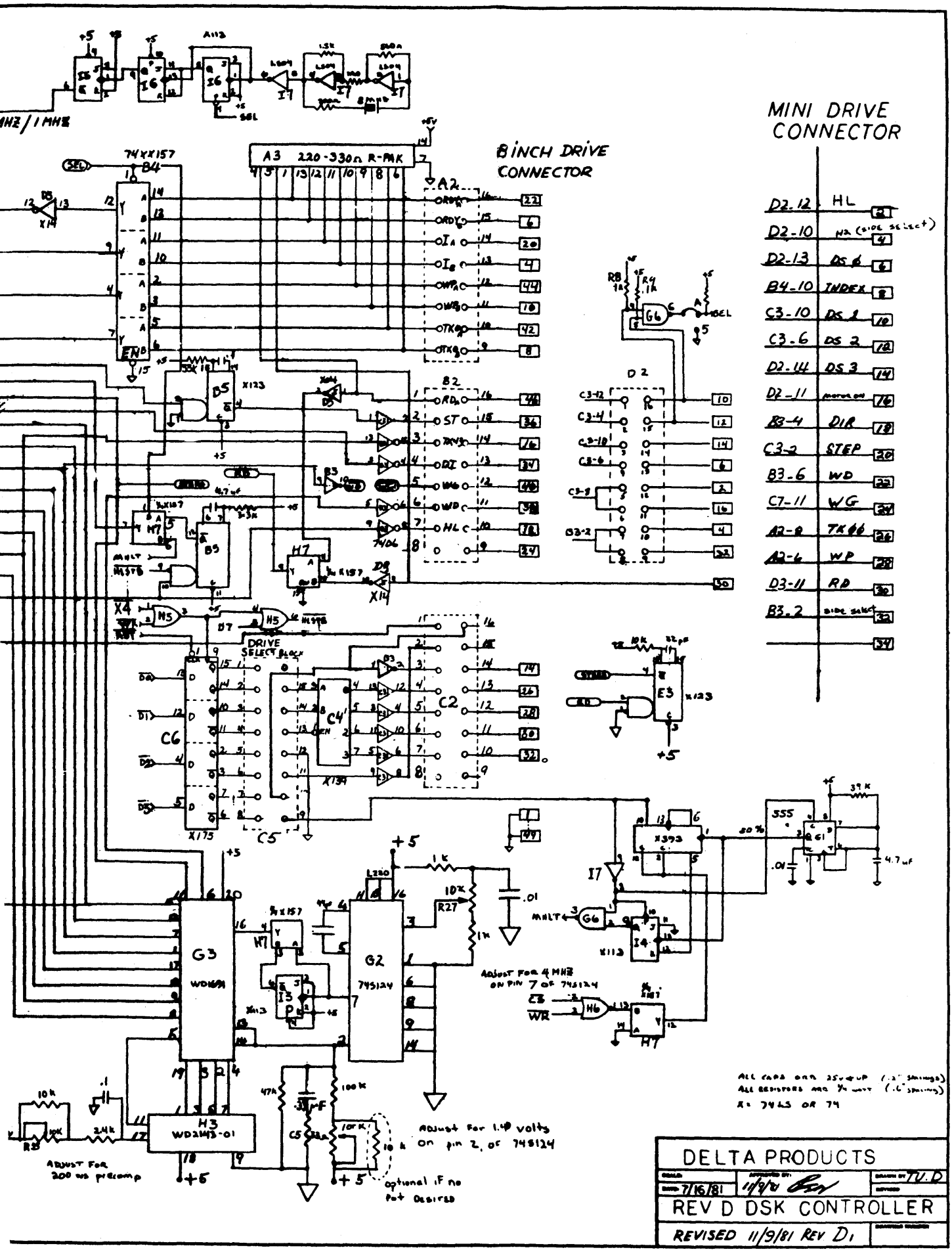
NOTES:

1. MARK ASSEMBLY P/N PER TABLE 1 IN AREA SHOWN.
2. MARK ASSEMBLY E.C. PER TABLE 1 IN AREA SHOWN.
3. P.C. BOARD FABRICATION MUST BE AT E.C. LEVEL 0775.
4. MAXIMUM COMPONENT HEIGHT IS 0.425".

MUST CONFORM TO ENGINEERING SPEC ES 3003-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO	TITLE TABLE ATE P.C.B. / SSE ASSY.
		6-79	1100	XEROX
		9-79	1132	DRAWN BB 4-79
CASE DEPTH	LINEAR .XX ± .010	1-80	1144	CHECKED
PLATING	.XXX ± .005	2-80	1222	APPROVED SIZE D SHEET 1 OF 1
SURFACE TREATMENT	ANGULAR ± 1°	6-80	1288	SCALE — SIZE D DWG NO 25074-2 REV 1288

VA800


XRDY
DI 7
VIO
SOUT
SINP
A2
A0
A1
PBIN
PWR
PRESET
A7
A6
A5
A4
A3
+5V
2MHZ / 1MHZ
INTRQ
RD
WR
DRQ
CS
MR
WR
ADJUST FOR
200 ns precomp


MINI DRIVE CONNECTOR
D2.12 HL
D2-10 HS (SIDE SELECT)
D2-13 DS 0
B4-10 INDEX
C3-10 DS 1
C3.6 DS 2
D2.14 DS 3
D2-11 MOTOR ON
B3-4 DIR
C3-2 STEP
B3-6 WD
C7-11 WG
A2-8 TK 00
A2-6 WP
D3-11 RD
B3.2 SIDE SELECT
8 INCH DRIVE CONNECTOR
A3 220-330Ω R-PAK
74XX157
DRIVE SELECT BLOCK
G3 WD1691
G2 74S124
H3 WD2143-01
Adjust for 4 MHz on pin 7 of 74S124
Adjust for 1.4 volts on pin 2 of 74S124
Adjust for 300 ns precomp
optional if no Pot Desired
ALL CAPS are 25V or up (.2" spacing)
ALL RESISTORS are ¼ watt (.4" spacing)
X = 74LS or 74
DELTA PRODUCTS
7/16/81
11/9/81
T.V.D
REV D DSK CONTROLLER
REVISED 11/9/81 REV D1