DELTA PRODUCTS DP-CPU-B ADDENDUM

As you will notice, DELTA PRODUCTS is in the process of changing our CPU design. The new product will be referred to as the DP-CPU-B.

Several changes in appearance will be noted. Please refer to the enclosed parts layout pictorial to orient yourself during the following paragraphs.

CHANGES THIS REV:

1. PROGRAMABLE BAUD RATE:

The 8116 can now be written into under software control of the Z-80 at Port 0BH to set the baud rate without removing the board from the computer. The lower 4 bits program the CPU-B serial channel A and the upper 4 bits program channel B. The old baud rate switch may be read through IO Port 0BH. The 1.83 DP monitor prom reads this 8 bit switch and loads the 8116 accordingly. Your boot or system initializations software may choose to use these 8 bits (or some part of them) to signal other things to the system.

2. POWER ON JUMPER DISABLE:

Jumper J9 when placed in the up position will cause the Z-80 to go to system RAM after a reset.

3. E PROM DISABLE:

Jumper J6 when placed in the left position will permnently disble the E Prom. When enabled the Prom may be used exactly as it has been in the past.

4. 2 MHZ/4 MHZ JUMPER:

The jumper (J2) enabling you to switch from 2 to 4 MHZ is now at the top of the board. See pictorial for new locations.

5. VECTORED INTERRUPT RESPONSE:

A header at the top of the board (11A) connects the various interrupt and timing capabilities of the Zilog CTC timer chip (11B) to their chosen destinations. Boards without a "B" designation on the back side of the board under the baud rate crystal do not have the CTC functions implimented yet and should be used as "A" boards as far as vectored interrupts or CTC functions are concerned.

6. IO PORT ADDRESSES:

The IO ports will be addressed at ports 0-F when Jumper J7 is in the right hand position, and 10H to 1FH when the Jumper is in the left hand position.

TABLE OF CONTENTS

An examination of any of these particular areas should answer most questions regarding the operation of the CPU.

If any additional questions should arise, please write the factory at:

DELTA PRODUCTS, INC.
15392 Assembly Ln.,
Huntington Beach,CA 92649
Tel: (714) 898-1492

Section 1.0

GENERAL DESCRIPTION

The DP CPU is a multipurpose control card designed to run on the S-100 buss with a minimum of additional circuitry.

The product was designed in 1977 and put into production with some modification in 1978. A typical business or personal computer system can be configured with only three cards and a motherboard.

1. DP CPU-A
   - Z80 Central Processor
   - 2 Serial Programmable RS-232 IO Ports
   - 1 8255 24 Bit Parallel IO Port
   - M1 Wait State for 160% thruput enhancement with 450ns memory
   - 2708 or 5 Volt 2716 Power on Jump Eprom
   - Memory Management on A16 & A17

2. DP 32K-A
   - 32K multi-addressable memory featuring additional address lines A16 & A17 for parallel or extended addressing to 256K

3. DP DSK-A
   - Single or double density floppy disk controller using WD-1791 LSI chip. Works with Shugart, Siemens, Calcomp, Persci, etc. single or double sided drives.

4. DP MTH-A
   - 10 Slot shielded S-100 motherboard. Measures 10 x 7.5 inches. Mounts on stand-offs or rails.

Section 2.0

SERIAL IO BAUD RATE SELECT

The ports for the Serial IO are:

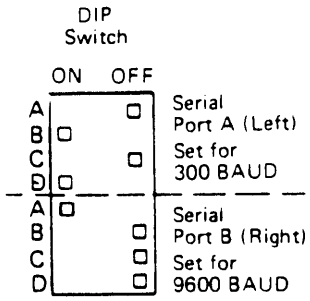
A Status = 1	A Data = Ø (on the left)
B Status = 3	B Data = 2 (on the right)

The 8 position DIP switch at the lower right hand corner of the board is broken into two 4 bit sections. The upper 4 bits select the IO baud for the left 8251 and the lower 4 bits select the baud for the right.

The switches are used in a binary pattern to set the rates as follows:

X = OFF O = ON

Baud	D	C	B	A
50	O	O	O	O
75	O	O	O	X
110	O	O	X	O
134.5	O	O	X	X
150	O	X	O	O
300	O	X	O	X
600	O	X	X	O



Baud	D	C	B	A	
1200	O	X	X	X	
1800	X	O	O	O	
2000	X	O	O	X	
2400	X	O	X	O	
3600	X	O	X	X	
4800	X	X	O	O	
7200	X	X	O	X	
9600	X	X	X	O	
19200	X	X	X	X	(Special Fast) (8251)

NOTE: Make sure when using the above chart that the positions we show correspond to the type of switch you have on the board. Some models of switches have the 'ON' to the opposite side.

The 8251 can be programmed under software control to do a number of things. A copy of the tech sheet on the chip can be found in the appendix. The following code can be used to initialize what might be a 'normal' mode for the 8251. (The chip must be initialized or it will do nothing.)

```
MVI A, ØAAH     ;Load A
OUT Ø3          ;Initialize Port B
OUT Ø1          ;Initialize Port A
MVI A, 40H      ;Load A
OUT Ø3          ;With Internal Reset
OUT Ø1          ;Write to Both Ports
```

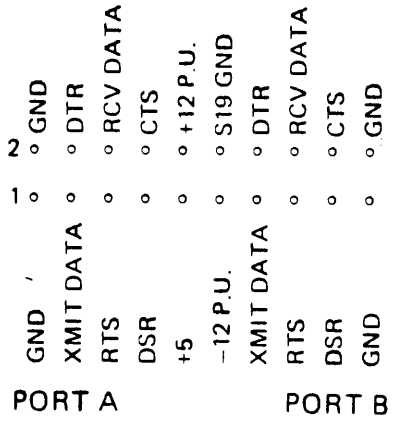
8251 Status Flags (when you input status port, this is what byte will mean):

Bit:	Ø7	Ø6	Ø5	Ø4	Ø3	Ø2	Ø1	Ø0	
	DSR	SY	FE	OE	PE	TXE	RXR	TXR	⇦ Output bit (RDY when Hi)
							⇧		Input bit (RDY when Hi)

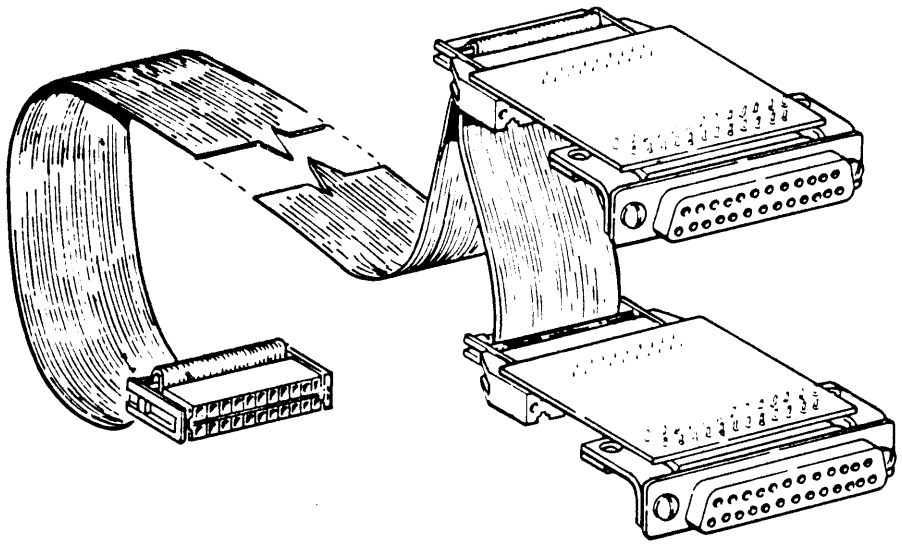
Section 2.2

PIN OUT OF SERIAL CONNECTOR

The pin out of the RS-232 connector (on the right) is as follows:



As an option we can supply a 26 pin ribbon connector with two connectors on one end and one on the other. When mated with a pair of our STOD PC boards a neat interface to a standard 'D' RS-232 connector (chassis mount) may be realized. The set up looks like this:



The cost of the above lash-up is $32.00. Sorry the price is high but if you will total the price on all the connectors (5) and the PC boards (2) plus the ribbon and labor, you will find it's the best that can be done.

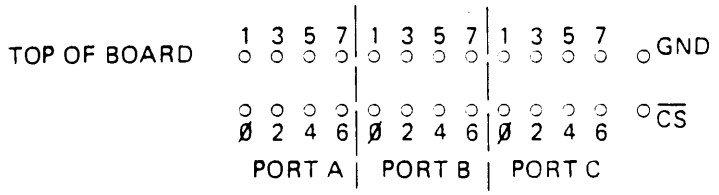
Section 3.0 and 3.2

PARALLEL INTERFACE AND PIN OUT OF PARALLEL CONNECTOR

Parallel 8255 IO Port.

The Ports decoded for operation are: Port A = Ø4H B = 05H C = 06H CMD = 07H

The Parallel 8255 pin-out is as follows:



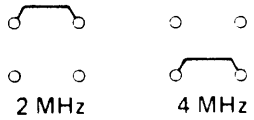
The 8255 chip tech sheet can be found in the appendix.

This chip is programmable in so many configurations that it is not possible to offer an adequate operational guide. Basically the device has three 8 bit ports, A, B, and C. A can be simultaneously input and output. B can be commanded to be an input or an output. C can be part in, part out or linked with A & B (4 bits each) for handshaking. We have included in the pinout the CS (chip select) line to the 8255. It may have some use in certain applications where buffers are remotely attached to the fairly weak output of the device.

Section 4.0

2 MHZ TO 4 MHZ JUMPER SELECT

The DP CPU will run at 2 MHz or 4 MHz, as selected by jumper J2. This jumper is to the right near the bottom of the board. Coordinates: 10-D

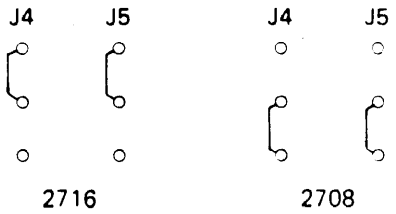


NOTE: The clock signal that appears on the bus is always 2 MHz, regardless of the speed at which the CPU is running.

Section 5.0

2716 TO 2708 EPROM SELECT

The DP Z80 CPU is designed for use with either a 2708 or a 5V only type of 2716 (Intel, Mostek). To select an Eprom move both jumpers J4 and J5 (near the top next to the 8255) to the upper position for a 2716 and to the lower position for a 2708.



The Eprom always occupies F800 – FFFF when enabled whether a 2708 or a 2716 is used.

If it is desired the DP CPU can be modified for use with the TI 2716 (+5V, -5V, +12V). The 2708/2716 jumpers should be in the 2708 position. Pins 18 and 20 are affected. Pin 18 is PD/PGM on the 5V part and CS on the TI part. Pin 20 is CS on the 5V part and A10 on the TI 2716. Therefore the following changes must be made on IC 8B.

From Pin	To Pin	
IC 8B 18	GND	Cut these traces at IC 8B
IC 8B 20	CS	
IC 8B 18	IC 9C p6	Install these jumpers on the back of the board
IC 8B 20	IC 5B p40	

Section 6.0

VECTORED INTERRUPT RESPONSE

The Z-80 CPU has three methods of responding to an interrupt. The DP CPU supports all three modes. They are: Model Ø, an instruction can be placed on the buss; Mode 1, restart to ØØ38H; Mode 2, upon initialization an upper page vector is loaded into the Z-80 I register. At interrupt response time, Z-80 will respond with an M1 + IOREQ (an impossible normal combination). At this time the lower page address (which will be added to the upper page previously stored in I register) should appear on the data buss. The Z-80 will use these two bytes to point to a software address where the address of the interrupt routine is to be found.

SECTION 7.0

POWER ON JUMP CIRCUIT

The DP CPU has an unusual and totally effective method of starting a computer after reset. Conceptually the 2708 or 2716 Eprom 'appears' at ØØØØH for the purpose of initializing the CPU. The Eprom may then be 'moved' to the last 2 K of ram and jumped to. What happens is the CPU executes a few instructions at ØØØØ, and jumps to itself at 62 K. It then does a 'read' of an IO port which changes the on-board addressing structure. After inputing port ØA the Eprom may only be read at F800, not every 2 K boundary as was the case before.

Here is some sample code that works:

```
ORGØF8ØØH

        JMP F803        ;These three bytes will be executed at ØØØØH
        IN ØAH          ;"Moves" Eprom, this is now F803
        MVI A, ØAAH     ;Load Accumulator
        OUT Ø3A         ;Initialize IO Port
                        ***JUMP TO RAM HERE***
        MVI A, Ø1H      ;Load Accumulator
        OUT Ø9H         ;Remove Eprom
```

The Eprom may be left in the computer memory space at 62 K at all times or removed by writing a Ø1H into IO Port 9. Writing a ØØH into IO Port 9 will bring it back. Ram and Eprom may exist simultaneously at either the initial ØØØØ reset location or at the subsequently directed F800 location. Memory writes or IO functions are not disturbed by the co-existence of the Eprom, only memory reads. By writing the correct code into Port 9, the Eprom may be toggled in and out disabling the ability to read from adjacent RAM.

The CPU is currently supplied without an Eprom to keep the cost low. If you should wish a program on a prom, we will burn one for a charge of $15.00 and supply the prom for an additional $10.00 (27Ø8). We will type in up to 50 Bytes of code for this amount. Any size program will be burned providing it is supplied to us on a CPM compatible disk as a Hex file. We will guarantee the burn but you must guarantee the code.

To disable Power On Jump to Eprom:

> Cut the trace from IC 13C, p 13 to IC 1ØC, p 11 (as shown) and install a jumper from pin 13, IC13 to ground (pin 7 on 13). With this modification, the Eprom can still be accessed normally from F8ØØH to FFFF Hex, and it can also be enabled through IO port ØA Hex.

Section 8.0

MEMORY MANAGEMENT CIRCUIT

Memory Management Lines A16 and A17.

The Proposed IEEE S-100 standard has assigned buss pins 16 and 17 to be extended address bits A16 and A17 respectively. The DP CPU has an on board IO latches decoded to enable setting these lines to enable parallel banks of memory.

The DP Mem 32K memory boards will respond to this type of memory management scheme enabling 256K to exist on any given S-100 buss with no conflict.

To set or reset the address lines A16 and A17 simply output the desired bit pattern on IO port ØBH. Bit Ø controls A16 and Bit 1 controls A17 and bits 2 through 7 are ignored.

Examples: To select the lowest 64K block of memory,

```
MVI A,ØØH
OUT ØBH        A16=Ø, A17=Ø
```

To select the highest 64K block of memory,

```
MVI A,Ø3H
OUT ØBH        A16=1, A17=1
```

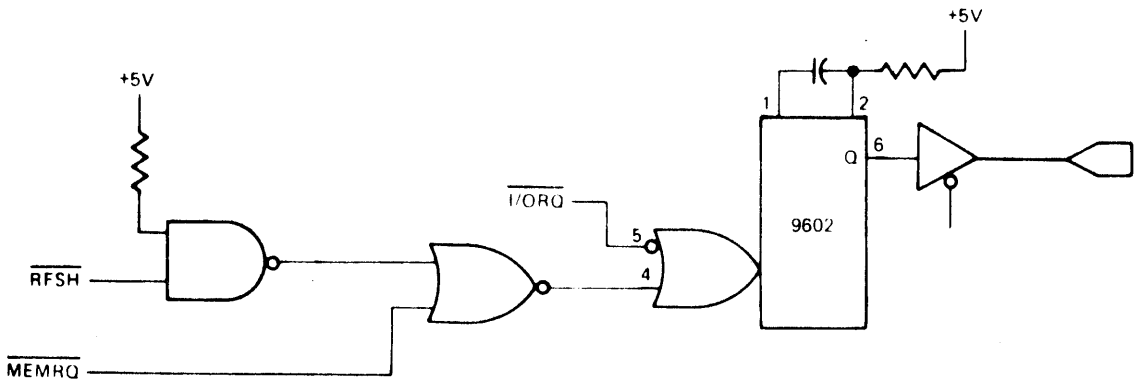
NOTE: A16 & A17 must be initialized in software to the desired levels after each system reset.

Section 9.0

P-SYNC GENERATOR

P-SYNC is a signal output by an 8080 to indicate that CPU status can be latched off the data bus.

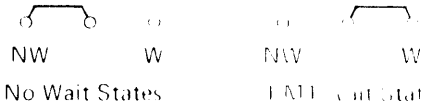
This signal is not produced on the Z80, and therefore must be simulated in order to make a CPU S-100 compatible. This is done as accurately as possible by generating a P-SYNC on every $\overline{MREQ}$ that is not a $\overline{RFSH}$ and on every I/O operation. This circuitry is provided on the DIR Z80 CPU.



Section 10.0

WAIT STATE ON M1 CIRCUIT

Jumper J1 allows the user to insert Ø or 1 wait state to each instruction fetch (M1) cycle. J1 is located in the left third of the board near the top.



To get the best system performance at a low cost, it is highly advisable to run the CPU at 4 MHz with 450ns memory and one M1 wait state. The M1 wait state adds only one clock cycle (250ns) to each instruction and the shortest instruction is four clock cycles long. Therefore, the worst case improvement in system throughput is 160%, with a typical speed improvement of about 180%.

Section 11.0

DELTA PRODUCTS MONITOR

Upon reset the CPU will initialize port 10 Port 2 and sign on. It will start at ØØØØ, locate top of RAM and put its stack there. The DP monitor will respond to the following commands:

D = DUMP
Enter beginning address, ending address. A beginning address and a 'CR' will display 15 lines automatically. A 'CR' for a beginning address will enter ØØØØ.

L = LOAD
Enter beginning address. 'CR' steps through memory. A '.' (period) stops entry.

M = MOVE
Enter source address, destination address, block length in Hex.

F = FILL
Enter starting address, ending address, character to fill.

V = VIEW
ASCII Dump to Monitor. + up one line, - down one line, 'CR' = 512 Bytes, Space bar = out.

G = GO
Enter destination address.

H = HEX STRING LOCATE
Enter starting address, ending address, string to locate.

SPECIALS: (* = not in 2708 [1K] version)

* R = READ
Cassette, Tarbell format. Enter destination address, block length in 1/4 K (255 Byte) segments. Will report "E" if checksum error.

* W = WRITE
Write to cassette, Tarbell format. Enter source address, block length in 1/4 K (255 Byte) segments. "W" will appear after write.

Control 'C' will execute Tarbell type floppy disc boot routine. Failure to boot will fall into trace function with error code in register A. (1 K version will report only 1771 error.)

* TRACE TYPE register dump may be enabled by placing a JMP to F815 (C3 15 F8) at 0038. Place a FF at the location in the program where the break-point is desired. In the act of executing a RST (ØFFH) the CPU will push the current program counter onto the stack. It will be recovered by the trace routine and printed on the screen.

The following is an Entry jump table at the beginning of the prom:

```
F800  C3 XX XX  JMP MONINZ  ;INITIALIZE ROUTINE
F803  C3 XX XX  JMP MONTR   ;MONITOR W/O INIZ
F806  C3 XX XX  JMP CONIN   ;CONSOLE INPUT ROUTINE
F809  C3 XX XX  JMP CONOUT  ;CONSOLE OUTPUT ROUTINE
F80C  C3 XX XX  JMP LIST    ;PRINTER DRIVER
F80F  C3 XX XX  JMP CASIN   ;TARBELL CASSETTE
F812  C3 XX XX  JMP CASOUT  ;TARBELL CASSETTE
F815  C3 XX XX  JMP TRACE   ;TRACE OUTPUTS REGS ON SCREEN
F818  C3 XX XX  JMP CONST   ;KEYBOARD STATUS
F81B  C3 XX XX  JMP INHX    ;HEX INPUT TO BINARY [A REG]
F81E  C3 XX XX  JMP OUTHX   ;BINARY TO HEX OUTPUT [B REG]
F821  C3 XX XX  JMP INADR   ;2 HEX BYTES TO BINARY [H&L]
F824  C3 XX XX  JMP ADOUT   ;ADDRESS TO CONOUT [H&L]
```

Note:

Version 1.82 and later of the DP monitor will sign on with a Hex address on the last line.

This is where the monitor has put its stack. If this address is less than the top of your current memory size, the monitor has encountered an error at that location. The monitor reads a Byte starting at Zero, compliments it, writes it out, reads it and compares it to what it wrote, if same it writes original byte back and goes on. When it detects write errors it puts its stack there, assuming it has found the top of Ram.

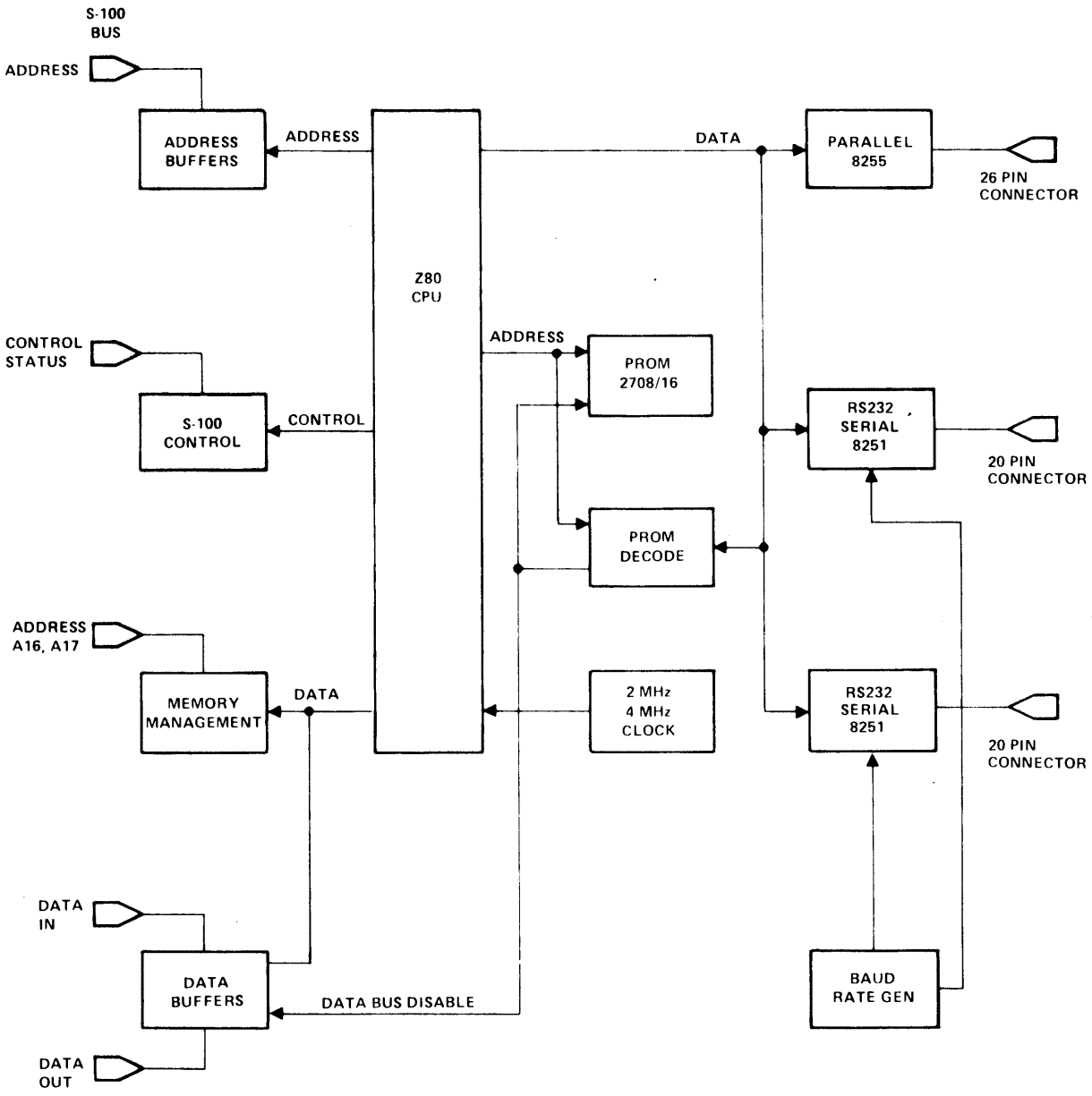
Filling memory with 55 Hex or AA Hex and resetting will do a quick and dirty alternate bit memory test.

Version 1.83 in later will output a constant string of Asterisks if it can find no memory.

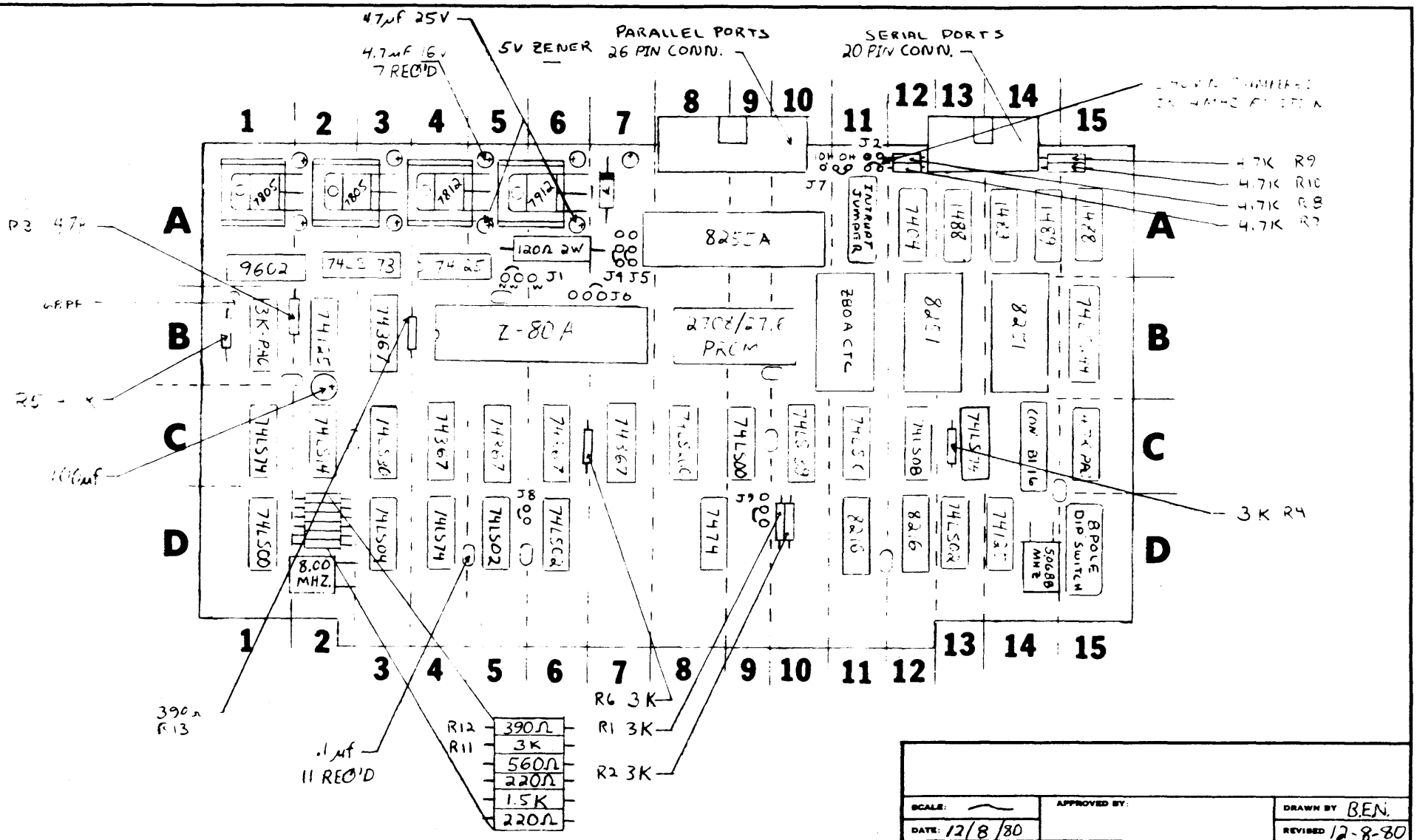
Section 12.0

DEDICATED ON BOARD IO PORTS

Port	Function	R/W
0	UART A, Data	(RW)
1	UART A, Status, CMD	(RW)
2	UART B, Data	(RW)
3	UART B, Status, CMD	(RW)
4	8255 A	(RW)
5	8255 B	(RW)
6	8255 C	(RW)
7	8255 CMD	(W)
8	Memory Management	(W)
9	Enable/Disable Prom	(RW)
A	Reset Address Decode	(RW)
B-F	(Unavailable to off board use)	



BLOCK DIAGRAM


47µf 25V
4.7µf 16V
7 REQ'D
5V ZENER
PARALLEL PORTS
26 PIN CONN.
SERIAL PORTS
20 PIN CONN.
4.7K R9
4.7K R10
4.7K R8
4.7K R7
3K R4
R3 4.7K
25 - K
100µf
390Ω R13
.1µf
11 REQ'D
R12 390Ω
R11 3K
560Ω
220Ω
1.5K
220Ω
R6 3K
R1 3K
R2 3K
8.00 MHZ.
Z-80A
8255A
Z80A CTC
8.0 MHZ.
8 POLE DIP SWITCH
SCALE:
APPROVED BY:
DRAWN BY B.E.N.
DATE: 12/8/80
REVISED 12-8-80 BY DAVE R.
Z80 CPU
CPU-B1
DRAWING NUMBER

Z80 CPU PARTS LIST

PART NO.	DESCRIPTION	QTY	LOCATING COORDINATES
CP100	BOARD	1	
8251	IC	2	B11-15
8255	IC	1	A8-10
Z80A	IC	1	B4-7
STD4	4MHZXTAL	1	D2
STD506	XTAL	1	D14
6073B	HEATSINK	4	A1-6
7805	REG	2	A1-2
7812	REG	1	A4
7912	REG	1	A6
609-2002	ANSLEY	1	A13
609 2602	ANSLEY	1	A9
341808	SWITCH	1	D13
950CP	PIN	7	
3.9KRES	RES	4	A13
.1BYCAP	CAP	17	D5
475MT	TANT	9	A1-7
150-2RES	RES	1	A6
47KRES	RES	1	B2
390RES	RES	1	D2
3KRES	RES	1	D2
560RES	RES	1	D2
220RES	RES	2	D2
1.5KRES	RES	1	D2
19620	TANTCAP	1	B2
440SCR	SCREW	4	A1-4
440NUT	NUT	4	A1-4
1N3826	DIODE	1	A7
314A302	RPAK	1	B1
314A472	RPAK	1	C15
COM5016	IC	1	D15
8216	IC	2	D11,12
7404	IC	1	D3
7402	IC	2	D5,D6
74LS74	IC	3	C1,C13,C14
74LS00	IC	2	D1,C9
7408	IC	1	C12
74LS10	IC	1	C11
74LS139	IC	1	C10
74LS260	IC	1	C8
74367	IC	5	B3,C4-7
7430	IC	1	C3
74LS14	IC	1	C2
74125	IC	2	A4,B2
MC1488	IC	2	A11,15
MC1489	IC	2	A12,14
40PSOC	SOCKET	1	
28PSOC	SOCKET	2	
16PSOC	SOCKET	9	
24PSOC	SOCKET	1	
14PSOC	SOCKET	22	
18PSOC	SOCKET	1	
8602	IC	1	A2
7474	IC	1	D4
929834-01R	1X36 AP	1	
4.7KRES	RES	1	A1
CK68PF	CAP	1	A2

APPENDIX A

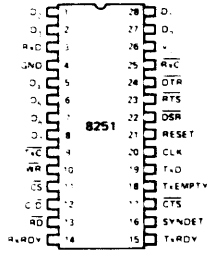
intel

8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1, 16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous Asynchronous Receiver Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology

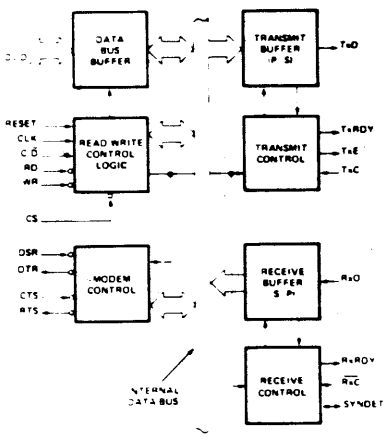
PIN CONFIGURATION



Pin Name	Pin Function
D0-D7	Data Bus (8 bits)
C/D	Control or Data (Used for Write or Read)
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (Has character for 8080)
TxRDY	Transmitter Ready (Ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is general purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

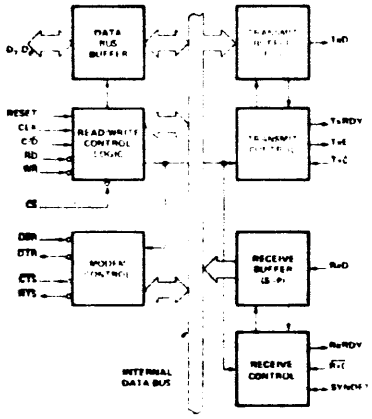
TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for the Polled operation the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go "high". It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxE is independent of the TxEN bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers". TxE goes low as soon as the SYNC is being shifted out.



$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System its functional configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset)

A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition. Minimum RESET pulse width is 6 t_{CY}.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{WR}$ (Write)

A "low" on this input informs the 8251 that the CPU is outputting data or control words, in essence, the CPU is writing out to the 8251.

$\overline{RD}$ (Read)

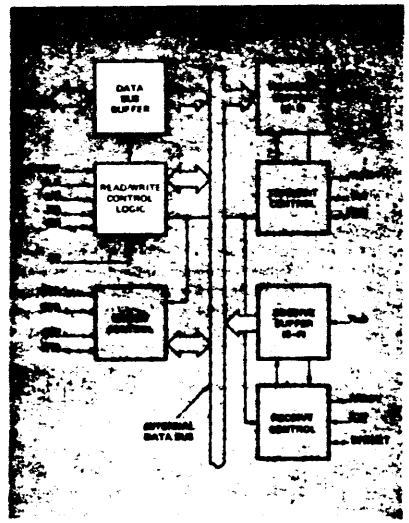
A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.



C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 → DATA BUS
0	1	0	0	DATA BUS → 8251
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3 STATE
X	X	X	1	DATA BUS → 3 STATE

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD PARITY etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device, upon receiving an entire character the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN(Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external)

The control words are split into two formats.

1. Mode Instruction
2. Command Instruction

Mode Instruction

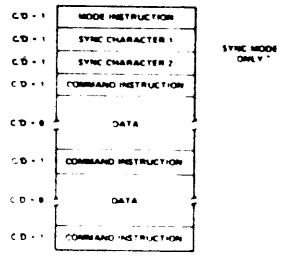
This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



Typical Data Block

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RxC}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{RxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier, it can be 1x, 16x or 64x the Baud Rate.

For Example: If Baud Rate equals 300 Baud,
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

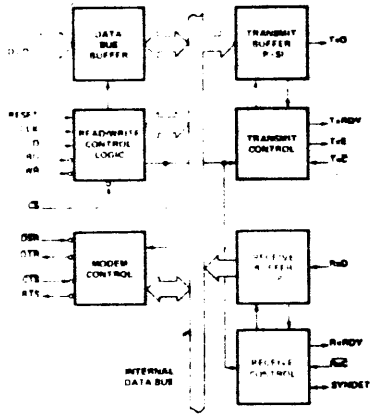
Data is sampled into the 8251 on the rising edge of $\overline{RxC}$.

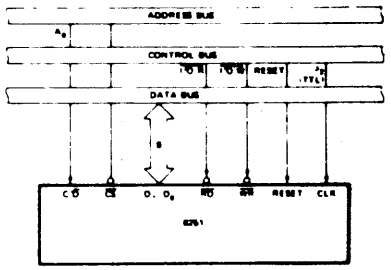
NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RxC}$.



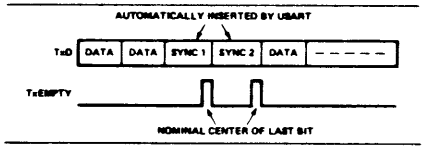


8251 Interface to 8080 Standard System Bus

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. TxEMPTY goes low when SYNC is being shifted out (See Figure below). The TxEMPTY pin is internally reset by the next character being written into the 8251.



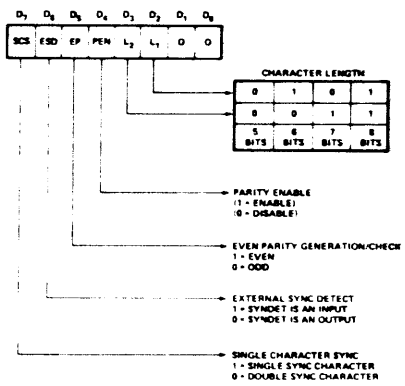
Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

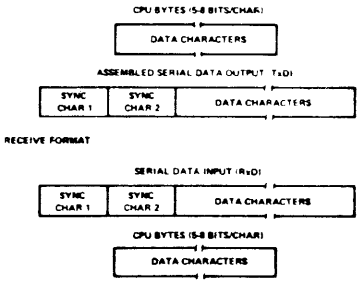
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.



Mode Instruction Format, Synchronous Mode



Synchronous Mode, Transmission Format

Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251 the designer can best view the device as two separate components sharing the same package. One Asynchronous the other Synchronous. The format definition can be changed "on the fly" but for explanation purposes the two formats will be isolated.

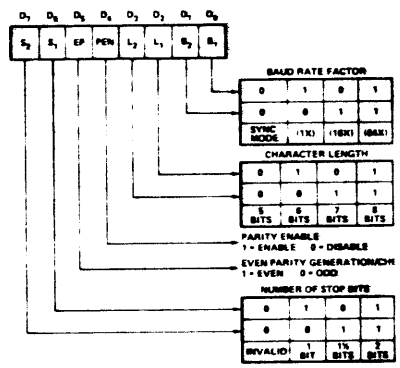
Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

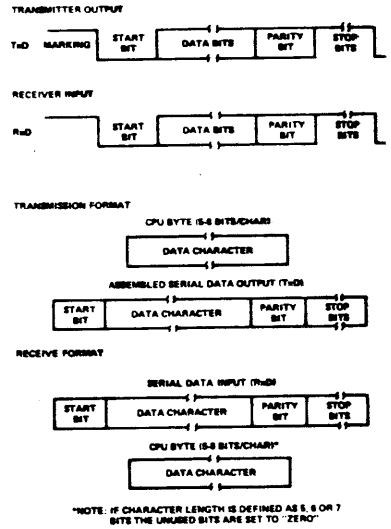
When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.

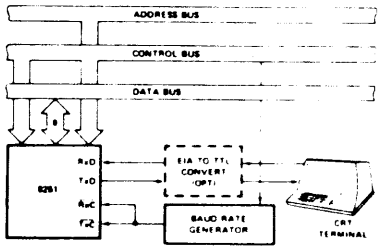


Mode Instruction Format, Asynchronous Mode

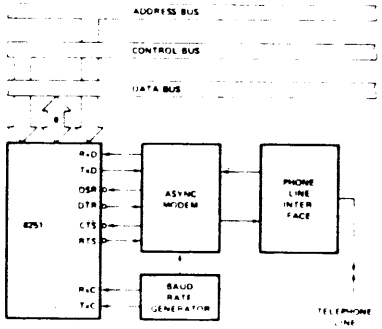


Asynchronous Mode

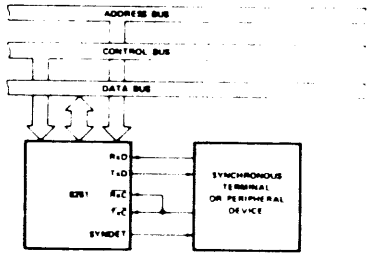
APPLICATIONS OF THE 8251



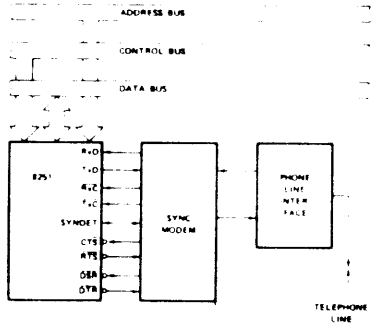
Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud



Asynchronous Interface to Telephone Lines



Synchronous Interface to Terminal or Peripheral Device

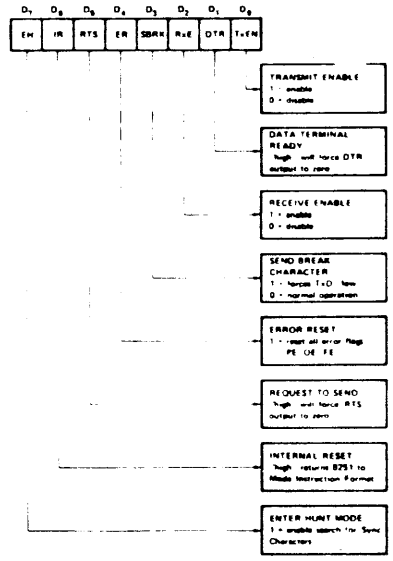


Synchronous Interface to Telephone Lines

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" (C/$\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.



Command Instruction Format

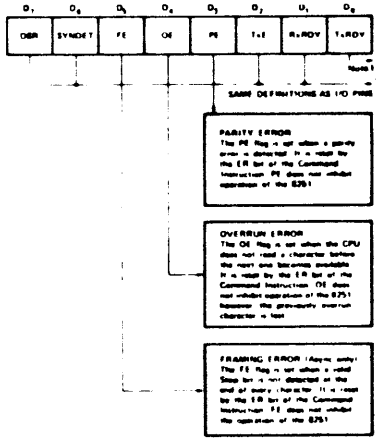
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation.

A normal "read" command is issued by the CPU with the C/D input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment.

Status update can have a maximum delay of 16 clock periods.



Status Read Format

Note 1 TxRDY status bit has similar meaning as the TxRDY output pin. The former is not conditioned by CTS and TxEN, the latter is conditioned by both CTS and TxEN
i.e. TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty · CTS · TxEN

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/D)	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/D)	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	430		ns	
t_{RD}	Data Delay from $\overline{READ}$		350	ns	C_L = 100 pF
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	C_L = 100 pF
		25		ns	C_L = 15 pF
t_{RV}	Recovery Time Between WRITES (Note 2)	6		t_{CY}	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	

NOTES: 1. AC timings measured at V_{OH} = 2.0, V_{OL} = .8, and with load circuit of Figure 1.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absol Maximum Ratings" may cause permanent damage to device. This is a stress rating only and functional op tion of the device at these or any other conditions ab those indicated in the operational sections of this spe cation is not implied. Exposure to absolute maxim rating conditions for extended periods may affect de reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			50	μA	V_{OUT} = .45V
				10	μA	V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

TEST LOAD CIRCUIT:

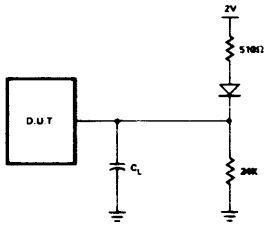
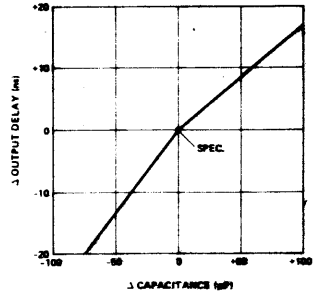
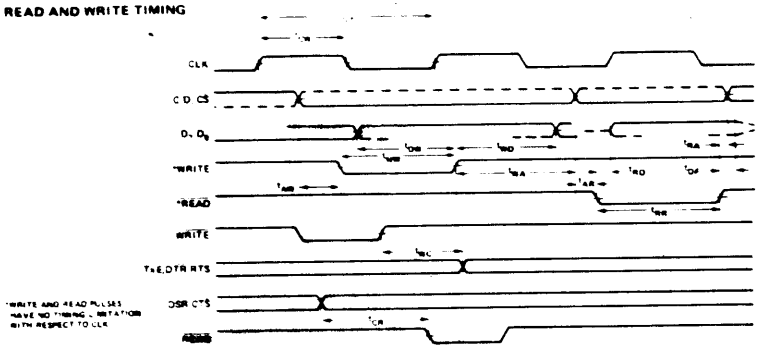


Figure 1.

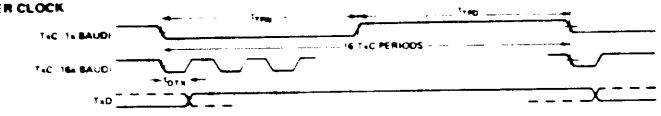
TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)



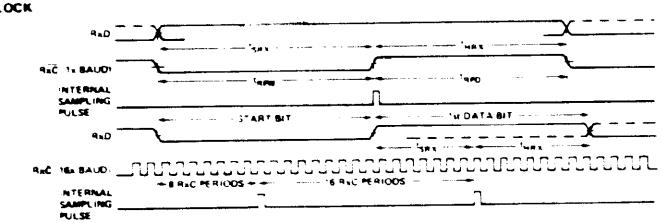
READ AND WRITE TIMING



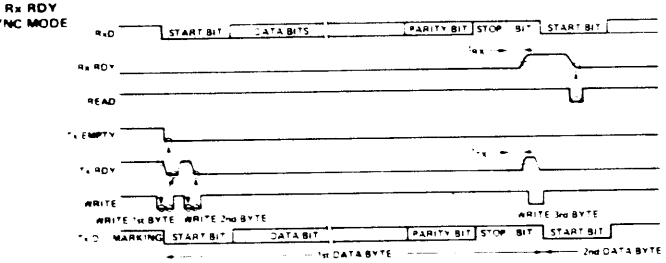
TRANSMITTER CLOCK AND DATA



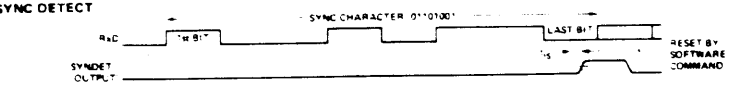
RECEIVER CLOCK AND DATA



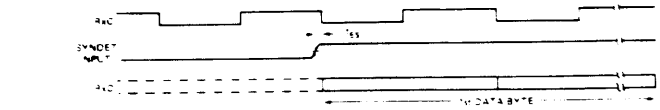
Tx RDY AND Rx RDY TIMING (ASYNC MODE



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



OTHER TIMINGS:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period (Note 3)	420	1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220	.7 t_{CY}	ns	
t_R, t_F	Clock Rise and Fall Time	0	50	ns	
t_{DTx}	TxD Delay from Falling Edge of TxC		1	μs	C_L = 100 pF
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	C_L = 100 pF
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	C_L = 100 pF
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{Tx}	TxRDY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{Rx}	RxRDY Delay from Center of Data Bit		20	t_{CY}	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		25	t_{CY}	
t_{ES}	Internal SYNDET Set-Up Time Before Falling Edge of RxC		16	t_{CY}	
t_{TxE}	TxEMPTY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{WC}	Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)		16	t_{CY}	
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		16	t_{CY}	

3. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate: t_{Tx} or $t_{Rx} > 1/30\ t_{CY}$
   For 16x and 64x Baud Rate: t_{Tx} or $t_{Rx} > 1/4.5\ t_{CY}$

4. Reset Pulse Width = 6 t_{CY} minimum

APPENDIX B

intel

IMPROVE

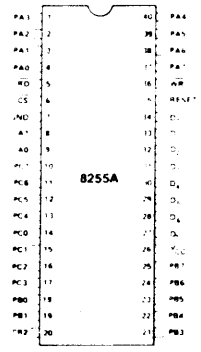
8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual-In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

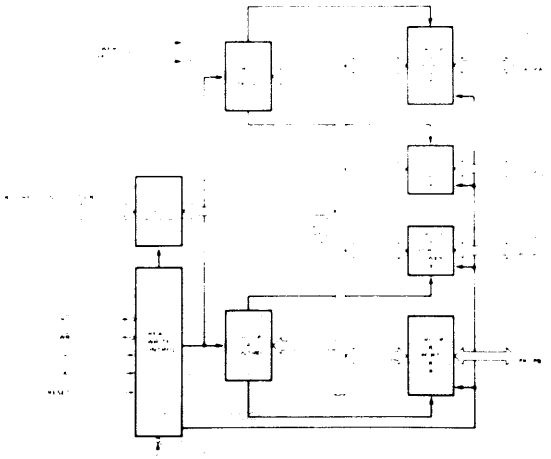
The 8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255A include bit set and reset capability, and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7 - D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

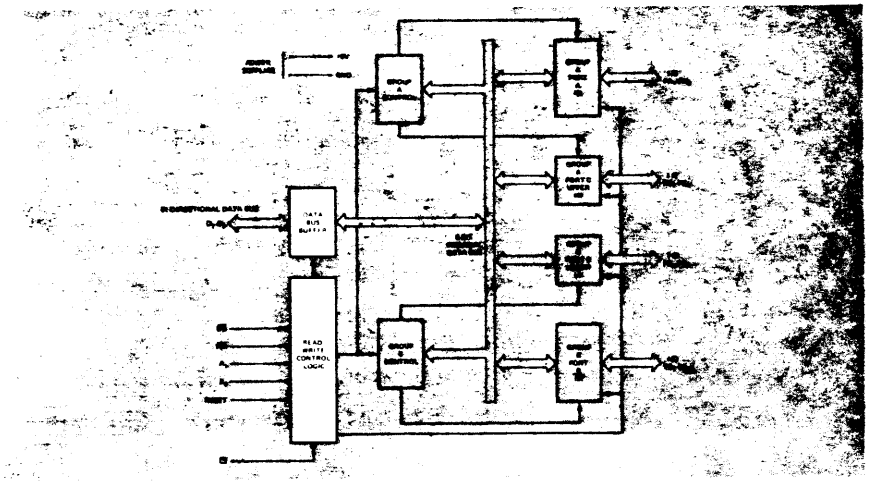
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE



8255 Block Diagram

(RESET)

Reset: A "high" on this input clears all internal registers including the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the 8080 CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

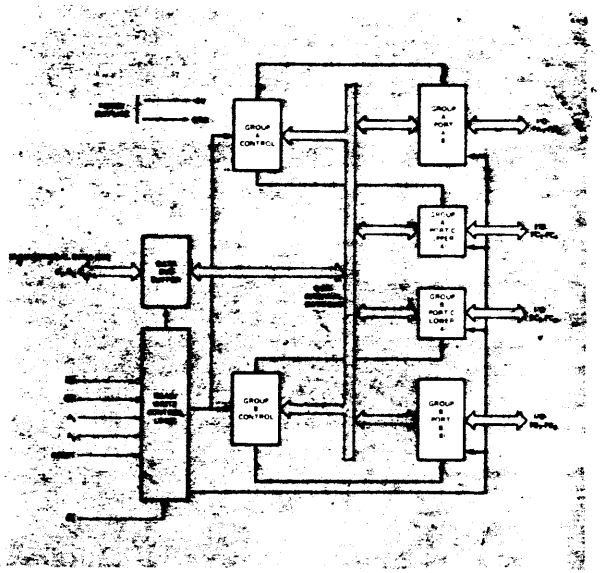
The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

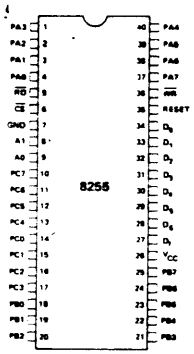
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

8255 BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

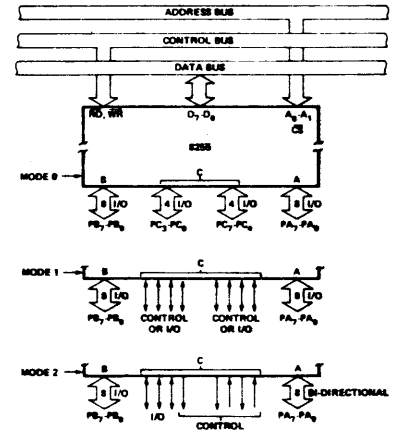
Mode Selection

There are three basic modes of operation that can be selected by the system software:

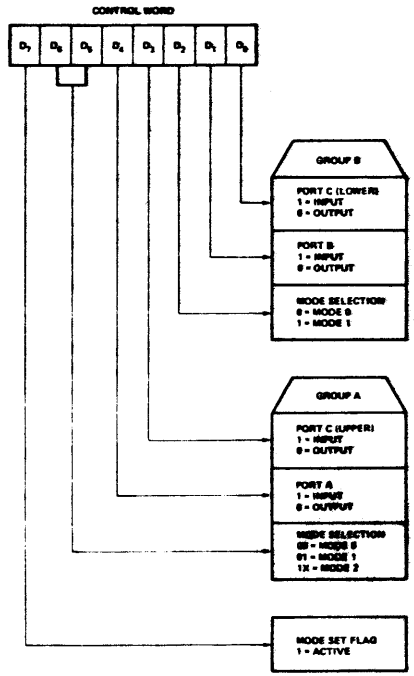
Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface

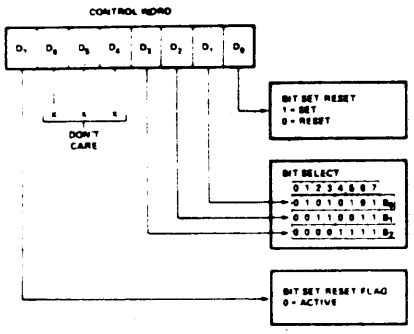


Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.



Bit Set/Reset Format

When Port C is being used as status control for Port A or B these bits can be set or reset by using the Bit Set Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and Device Reset.

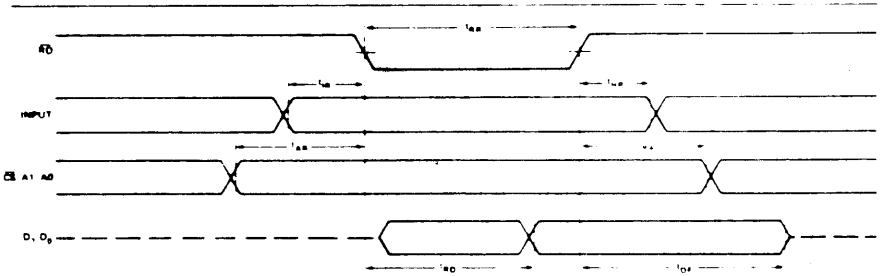
Operating Modes

Mode 0 (Basic Input/Output)

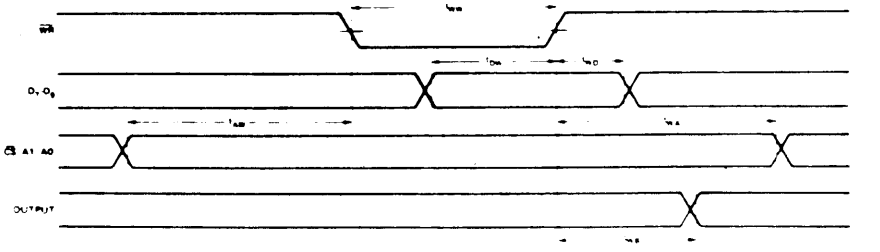
This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4 bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



Mode 0 (Basic Input)

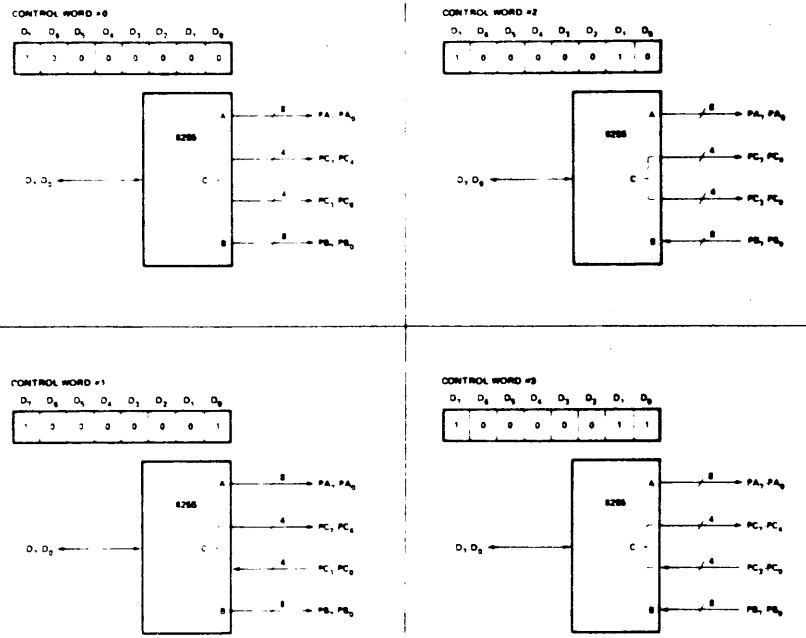


Mode 0 (Basic Output)

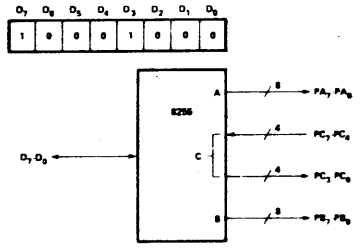
MODE 0 PORT DEFINITION CHART

A		B		GROUP A			GROUP B		
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

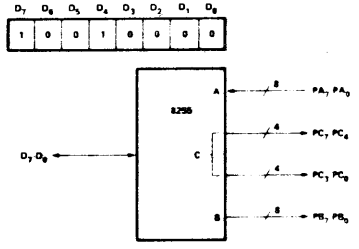
MODE 0 CONFIGURATIONS



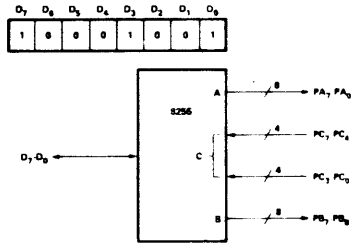
CONTROL WORD =4



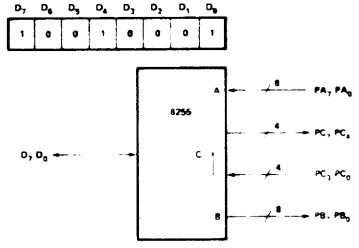
CONTROL WORD =8



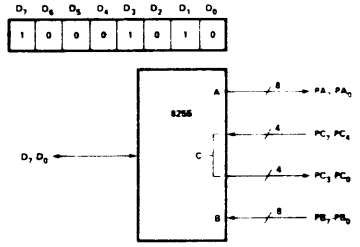
CONTROL WORD =9



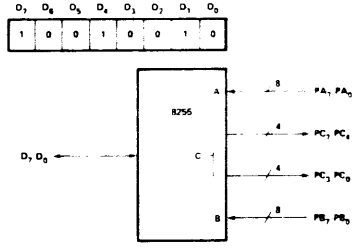
CONTROL WORD =9



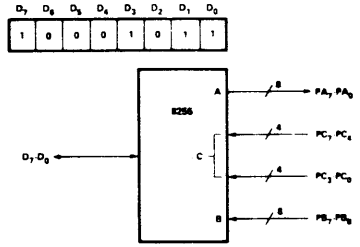
CONTROL WORD =6



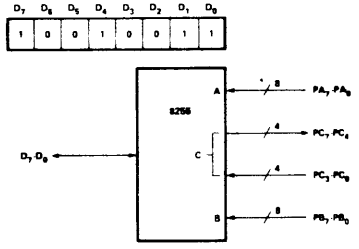
CONTROL WORD =10



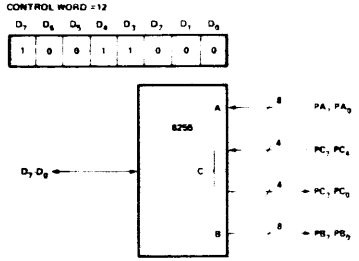
CONTROL WORD =7



CONTROL WORD =11



CONTROL WORD =12



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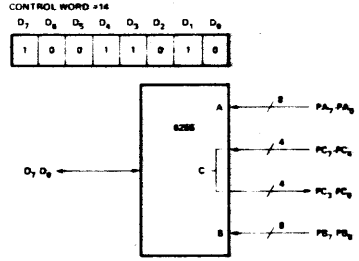
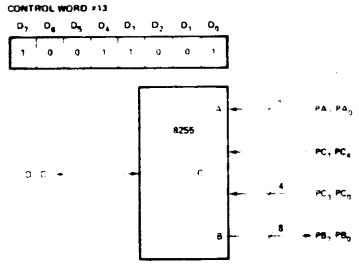
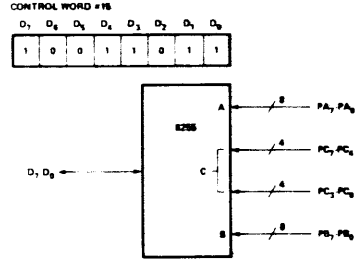


CONTROL WORD =13



CONTROL WORD =15



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

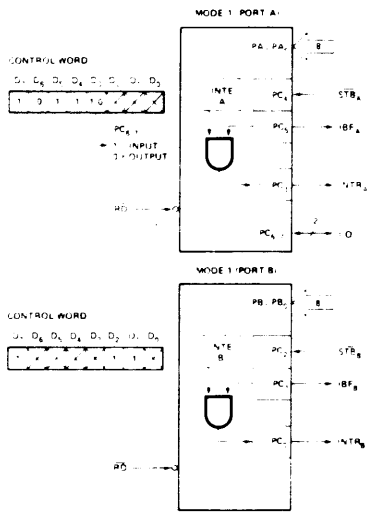
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

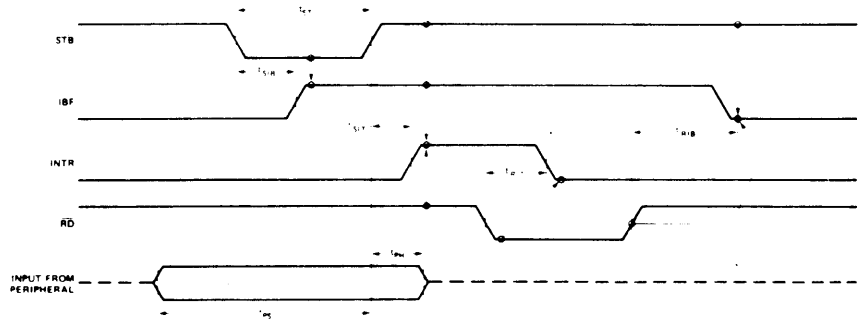
Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.



Mode 1 Input



Mode 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

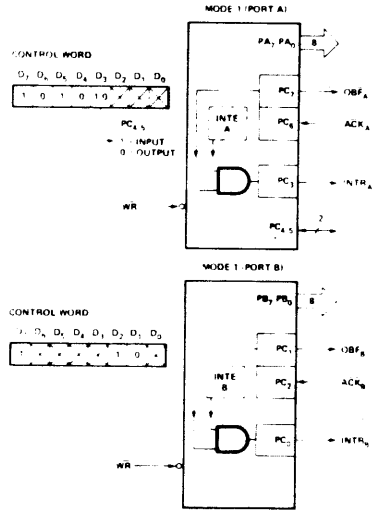
A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

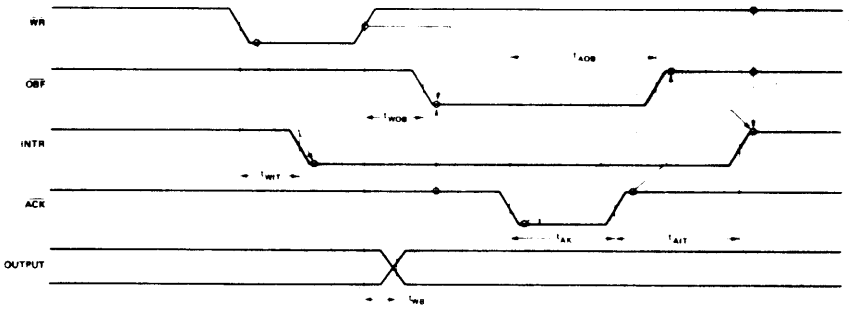
Controlled by bit set/reset of PC_6.

INTE B

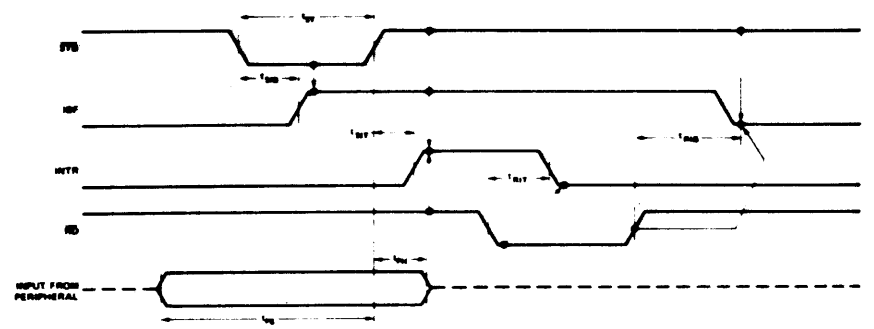
Controlled by bit set/reset of PC_2.



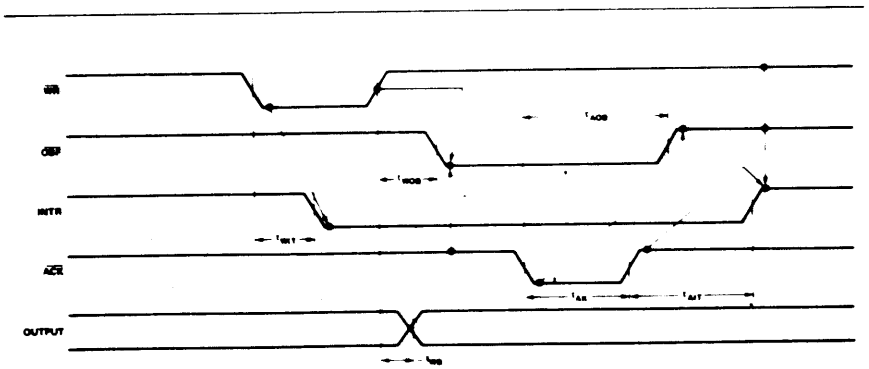
Mode 1 Output



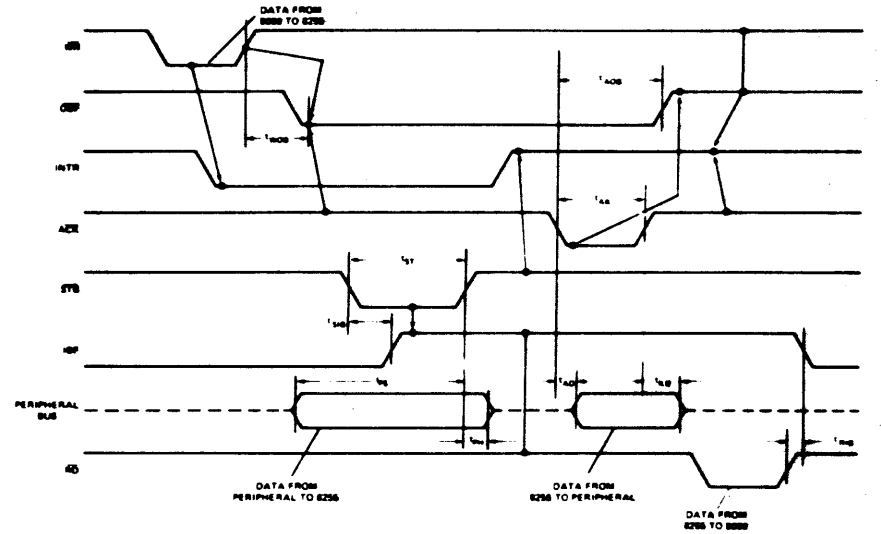
Mode 1 (Strobed Output)



Mode 1 (Strobed Input)



Mode 1 (Strobed Output)

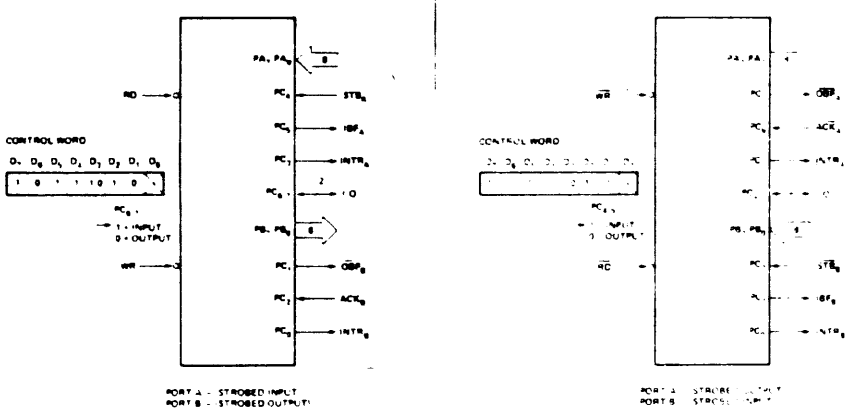


Mode 2 (Bi-directional)

NOTE Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.



Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

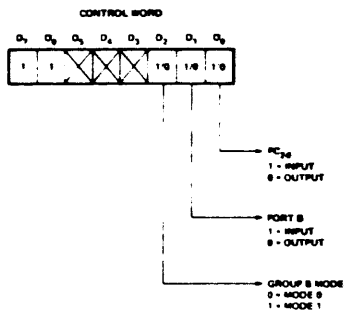
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

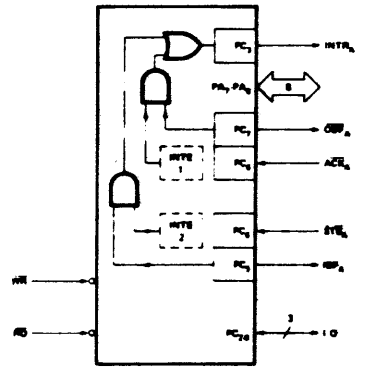
A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop associated with IBF)

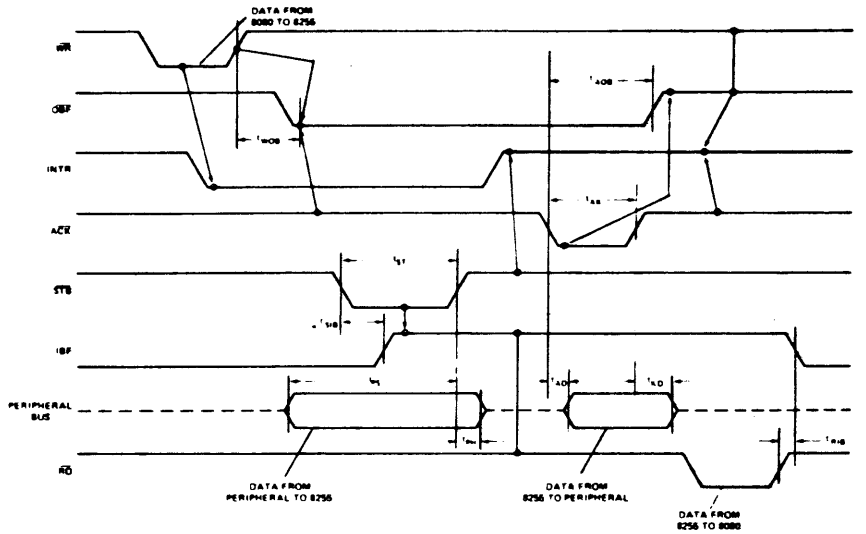
Controlled by bit set/reset of PC_4.



Mode 2 Control Word



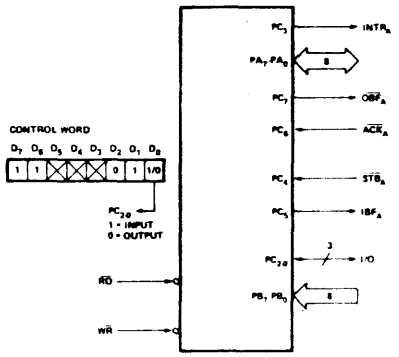
Mode 2



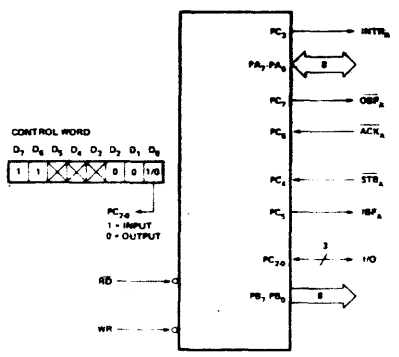
Mode 2 (Bi-directional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · MASK · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · MASK · $\overline{ACK}$ · $\overline{WR}$)

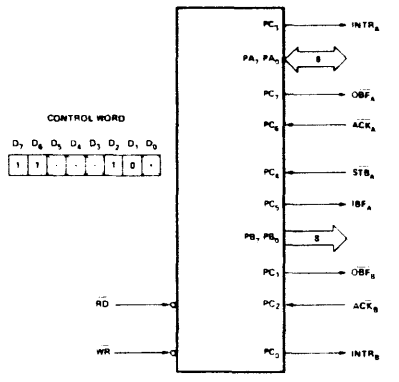
MODE 2 AND MODE 0 (INPUT)



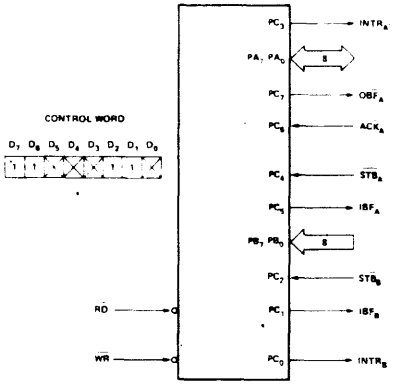
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



Mode 2 Combinations

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

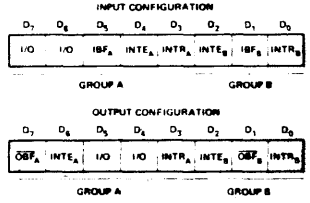
Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

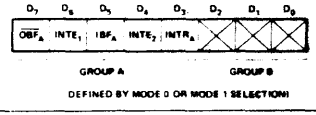
Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.



Mode 1 Status Word Format

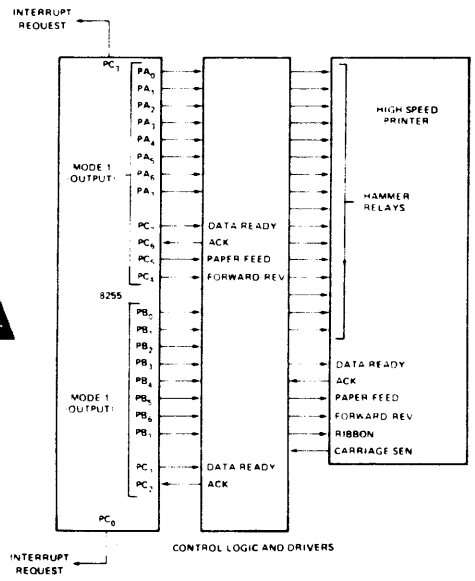


Mode 2 Status Word Format

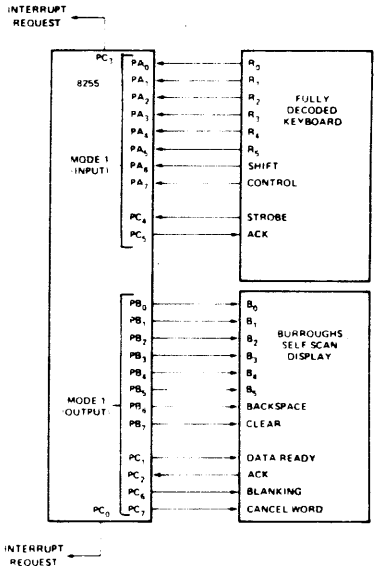
APPLICATIONS OF THE 8255

The 8255 is a very powerful tool for interfacing peripheral equipment to the 8080 microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

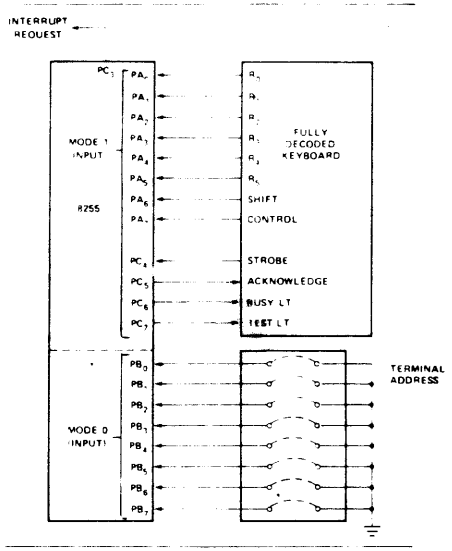
Each peripheral device in a Microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255 is programmed by the I/O service routine and becomes an extension of the systems software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the Detailed Operational Description, a control word can easily be developed to initialize the 8255 to exactly "fit" the application. Here are a few examples of typical applications of the 8255.



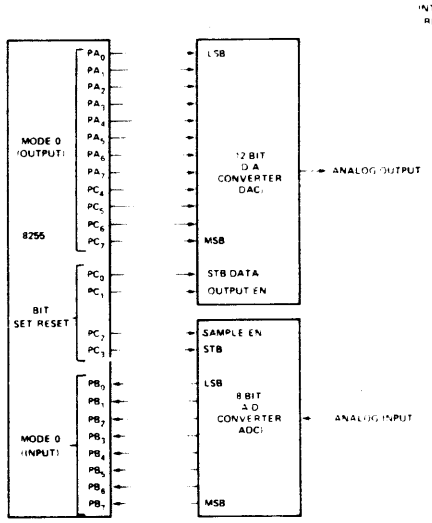
Printer Interface



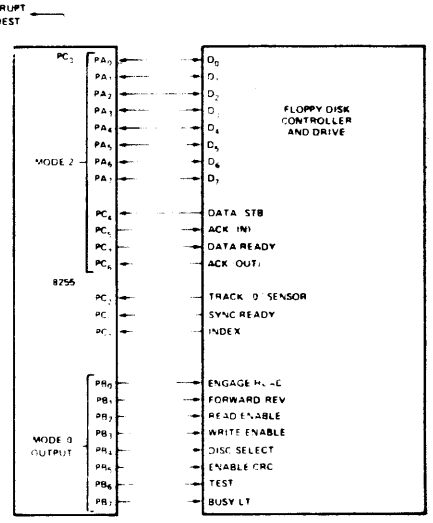
Keyboard and Display Interface



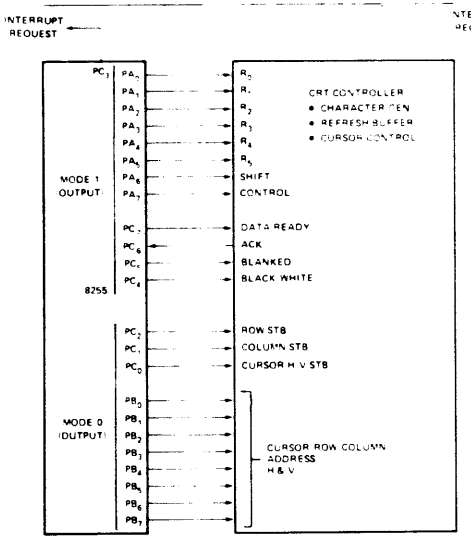
Keyboard and Terminal Address Interface



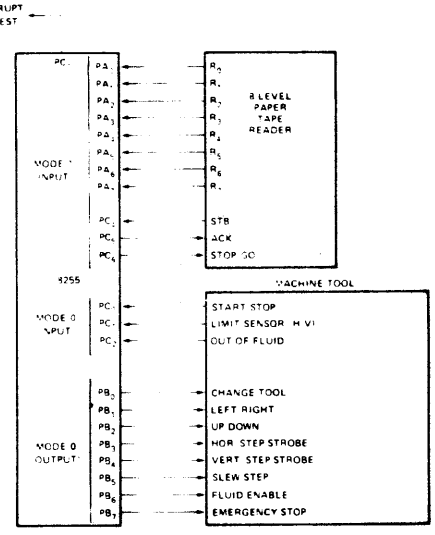
Digital to Analog, Analog to Digital



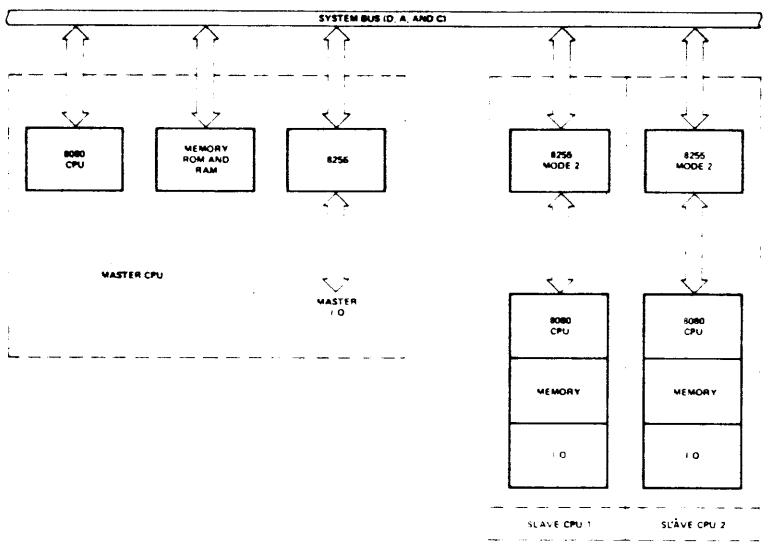
Basic Floppy Disc Interface



Basic CRT Controller Interface



Machine Tool Controller Interface



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65 C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%, GND = 0V

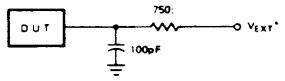
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
I_{OL}(DB)	Output Low Current (Data Bus)	2.5		mA	V_{OL} = 0.45V
I_{OL}(PER)	Output Low Current (Peripheral Port)	1.7		mA	V_{OL} = 0.45V
I_{OH}(DB)	Output High Current (Data Bus)	-400		μA	V_{OH} = 2.4V
I_{OH}(PER)	Output High Current (Peripheral Port)	-200		μA	V_{OH} = 2.4V
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω, V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC}
I_{OFL}	Output Float Leakage		10	μA	V_{OUT} = GND + 0.45, V_{CC}

Note: 1. Adaptable on any 8 pins from Ports B and C.

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT (FOR DB)



* V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%; GND = 0V

BUS PARAMETERS:

READ:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$	0		ns	
t_{RA}	Address Stable After $\overline{READ}$	0		ns	
t_{RR}	$\overline{READ}$ Pulse Width	300		ns	
t_{RD}	Data Valid From $\overline{READ}$		250	ns	CL = 100 pF
t_{DF}	Data Float After $\overline{READ}$		150	ns	CL = 100 pF
		10		ns	CL = 15 pF
t_{RV}	Time Between $\overline{READ}$s and or $\overline{WRITE}$s	850		ns	

WRITE:

t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Stable After $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Valid To $\overline{WRITE}$ (T.E.)	100		ns	
t_{WD}	Data Valid After $\overline{WRITE}$	30		ns	

OTHER TIMINGS:

t_{WB}	$\overline{WR}$=1 To Output		350	ns	CL = 100 pF
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	300		ns	
t_{ST}	$\overline{STB}$ Pulse Width	500		ns	
t_{PS}	Per. Data Before T.E. Of $\overline{STB}$	0		ns	
t_{PH}	Per. Data After T.E. Of $\overline{STB}$	180		ns	
t_{AD}	$\overline{ACK}$=0 To Output		400	s	CL = 100 pF
t_{KD}	$\overline{ACK}$=1 To Output Float		250	ns	CL = 100 pF
		20			CL = 15 pF
t_{WOB}	$\overline{WR}$=1 To $\overline{OBF}$=0		650	ns	CL = 100 pF
t_{ACB}	$\overline{ACK}$=0 To $\overline{OBF}$=1		350	ns	CL = 100 pF
t_{SIB}	$\overline{STB}$=0 To IBF=1		300	ns	CL = 100 pF
t_{RIB}	$\overline{RD}$=1 To IBF=0		300	ns	CL = 100 pF
t_{RIT}	$\overline{RD}$=0 To INTR=0		400	ns	CL = 100 pF
t_{SIT}	$\overline{STB}$=1 To INTR=1		300	ns	CL = 100 pF
t_{AIT}	$\overline{ACK}$=1 To INTR=1		350	ns	CL = 100 pF
t_{WIT}	$\overline{WR}$=0 To INTR=0		850	ns	CL = 100 pF

Note: Period of reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.

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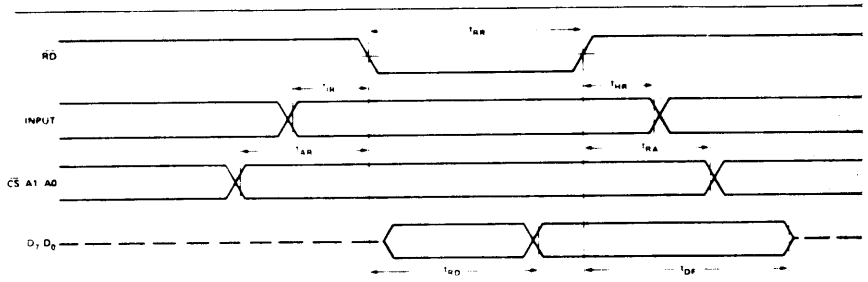
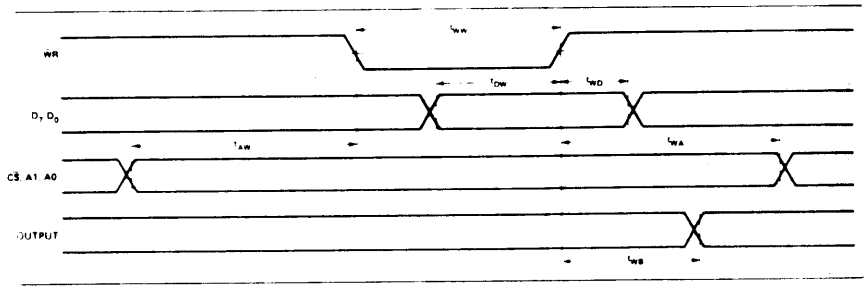
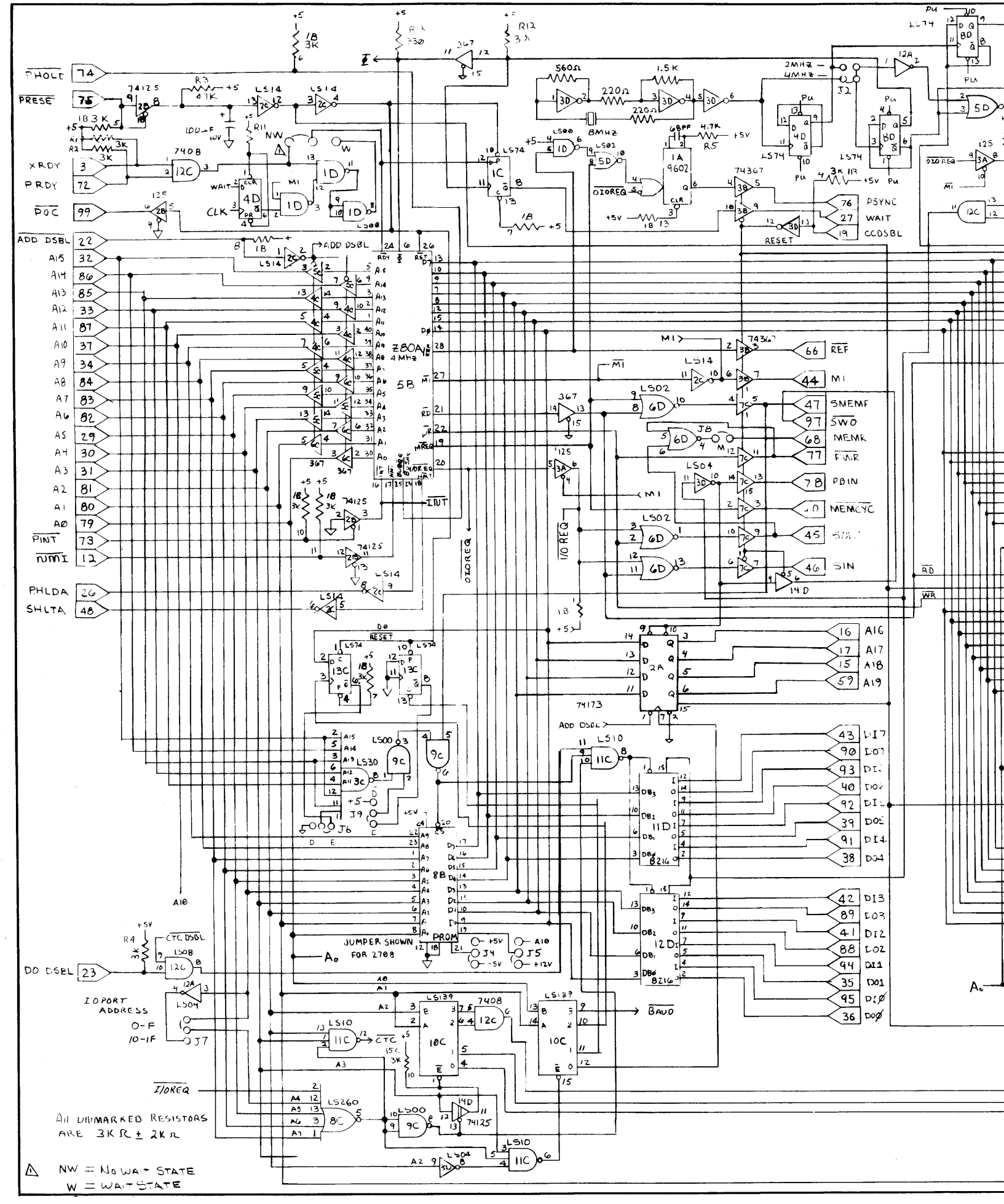
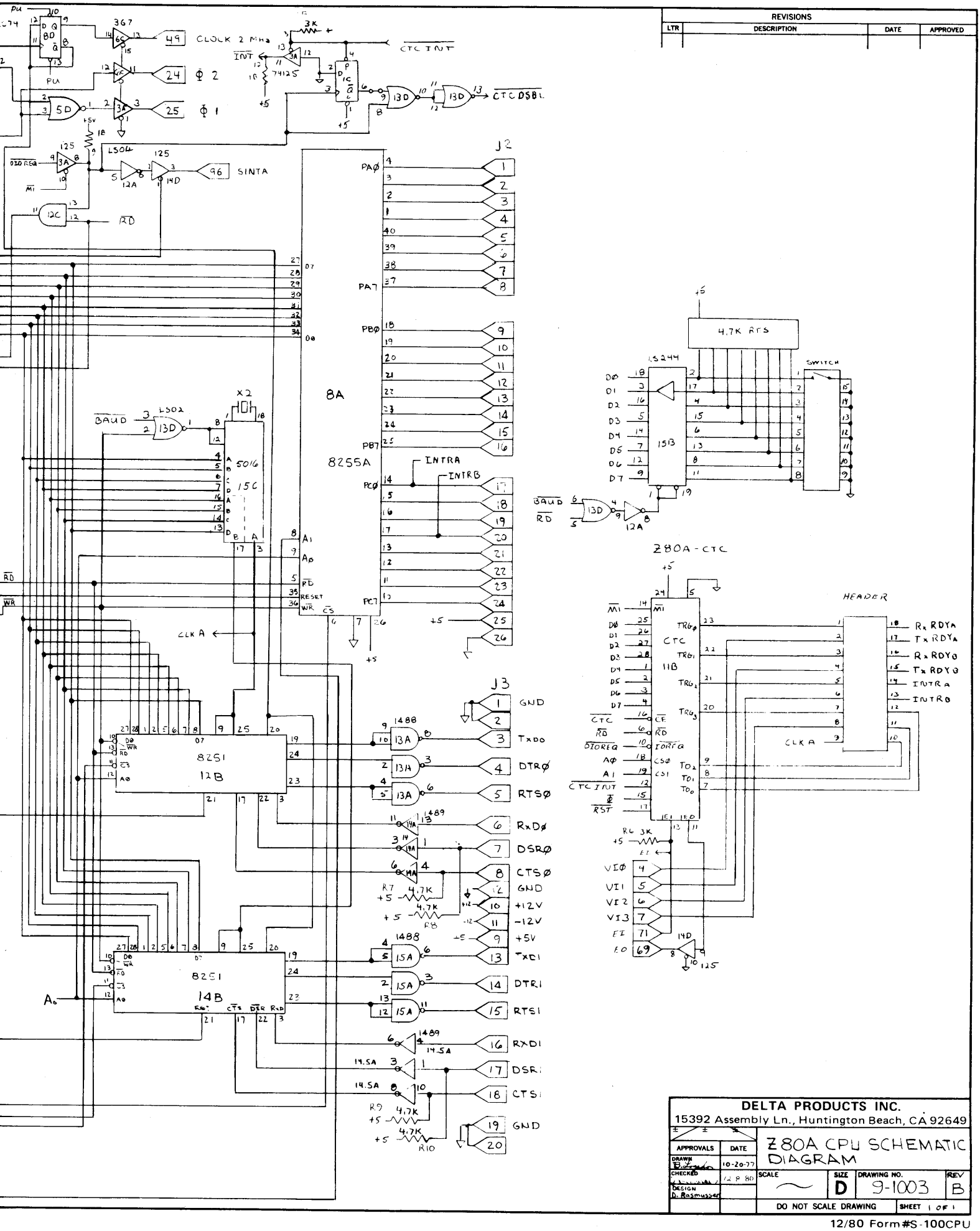


Mode 0 (Basic Input)



Mode 0 (Basic Output)


PHOLD 74
PRESE 75
XRDY 3
PRDY 72
POC 99
ADD DSBL 22
A15 32
A14 86
A13 85
A12 33
A11 87
A10 37
A9 34
A8 84
A7 83
A6 82
A5 29
A4 30
A3 31
A2 81
A1 80
A0 79
PINT 73
NMI 12
PHLDA 26
SHLTA 48
Z80A CPU 4 MHz
5B
INT
IOREQ
M1
RD
WR
MREQ
RESET
WAIT
CLK
2MHZ
4MHZ
8MHZ
PSYNC
WAIT
CCDSBL
REF
M1
SMEMF
SWO
MEMR
PWR
PBIN
MEMCYC
SOUT
SIN
A16
A17
A18
A19
DI7
DO7
DI6
DO6
DI5
DO5
DI4
DO4
DI3
DO3
DI2
DO2
DI1
DO1
DI0
DO0
74173
8216
PROM
JUMPER SHOWN FOR 2708
A10
DO DSBL 23
I/O PORT ADDRESS
0-F
10-1F
J7
BAUD
I/OREQ
ALL UNMARKED RESISTORS ARE 3K Ω ± 2K Ω
NW = NO WAIT STATE
W = WAIT STATE



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