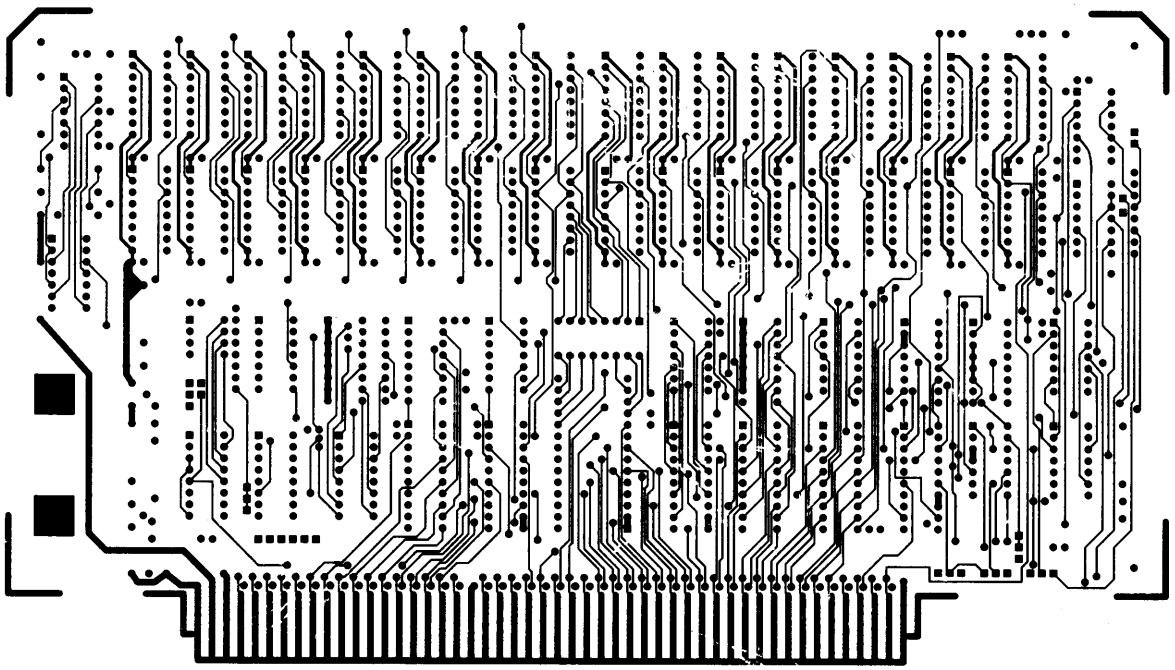
64K-DQ

OPERATION MANUAL



- FULLY BANK SELECTABLE
- I.O. PORT 40 (CROMEN CO) COMPATIBLE BANK SELECT
- DISABLE ON 16K BOUDNRIES
- ON BOARD REFRESH
- DMA COMPATIBLE
- EXTENDED ADDRESS LINES A16, A17, A18, A19
- FOUR LAYER CONSTRUCTION SUPER QUIET
- IEEE S-100

DELTA PRODUCTS

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DELTA PRODUCTS

Telex: 681-367 DELTMAR HTBH

DEALER:

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DELTA PRODUCTS

BOARD SELECT (MODE ONE) **********

I.O. port 40H may be written into, to select up to eight different boards. Each bit of the byte written to this port will represent a board selected. Only one bit may be set low at a time.

There is a relationship between the bits of dip switch SW2 and the bits of the byte written to I.O. 40. If you wish the board in question to be 'on' when data bit 0 is low, then the lowest switch of SW2 must be ON. If this board is to respond when data 03 is set low, switch 4 (counting up from the bottom) must be on.

EXAMPLES:

OFF	ON				
X		07			
X		06	F	E	(HEX)
X		05			
X		04	1111	1110	(BINARY)
X		03			
X		02			
X		01			
	X	00			
SW2			BYTE		

NOTE: Jumper E-4 E-5 (permanent enable) must be removed for I.O. port 40 select to work. Jumper E & B should be installed, T & S removed.

BOARD SELECT (MODE II) **********

S-100 EXTENDED ADDRESS lines A16 thru A23 (8 lines) are brought onto the board to switch SW1. The board may be selected by the logical comparing of the 8 bits of A16-A23 and the individual switches of SW1. Assume A16 to be switch one.

Note that this mode differs from I.O. port 40 select in that the switches here are set in a binary fashion, allowing two or more to be on at the same time. If two switches in I.O. 40 mode were on at the same time, there would be a data clash on the bus.

In this extended address mode the bits are decoded allowing up to 256 boards (?) to be separately addressed.

EXAMPLES:

	off	on	off	on	off	on	off	on
A16---	|	X|	|X	|	|	X|	|X	|
A17---	|	X|	|	X|	|X	|	|X	|
A18---	|	X|	|	X|	|	X|	|	X|
A19---	|	X|	|	X|	|	X|	|	X|
A20---	|	X|	|	X|	|	X|	|	X|
A21---	|	X|	|	X|	|	X|	|	X|
A22---	|	X|	|	X|	|	X|	|	X|
A23---	|	X|	|	X|	|	X|	|	X|
	0-64K		64K-128K		128K-192K		292K-256K	

NOTE: To enable extended address mode,
Jumper T-S must be removed and
Jumper E-B must be removed.

BANK DISABLE **********

This board is configured as 4 contiguous 16K memory banks. The banks are clearly marked BANK 0,1,2,3, on the artwork. Any 16K cell may be removed from responding when the rest of the board is selected by the appropriate setting of the bits on switch SW#. Bit switch 1 corresponds with bank number 3 (highest 16K) and switch number 2 is for the next lower bank.

EXAMPLES:

off	on	off	on	off	on	off	on
|	X|	|X	|	|	X|	|	X|
|	X|	|	X|	|X	|	|	X|
|	X|	|	X|	|	X|	|X	|
|	X|	|	X|	|	X|	|X	|
ALL BANKS ENABLED		48K-64K DIS-ABLED		32K-48K DIS-ABLED		0K-32K DIS-ABLED	

PHANTOM LINE **********

All memory banks will become disabled when S-100 bus pin 67 is pulled low. To disable this feature, cut the trace between F - H.

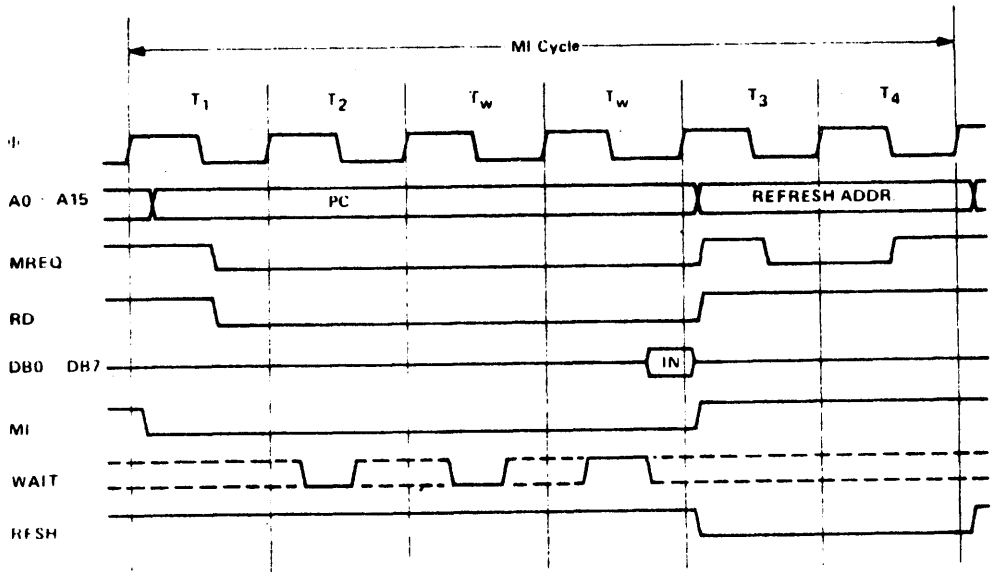
M-1 WAIT STATE GENERATION **********

In normal operation with a Z-80 CPU, no wait states will be generated.

There are certain asyncronous events that can cause the on board refresh circuitry to take over the job of periodically refreshing the dynamic memory chips. (i.e. DMA disk reads or other bus requests, or extended waits.)

When normal operation is resumed, (re-syncronization) a wait state may be automatically injected if the CPU should do a memory read while the board refresh circuitry is in midstate of a refresh cycle.

For further details of on/off board refresh timing, see theory of design and operation.



INSTRUCTION OP CODE FETCH WITH WAIT STATES

REFRESH CYCLE **********

A dynamic memory cell must be refreshed every 2ms. If not, the data bit in that cell will be lost. Refreshing a memory cell in a 4116 compatible RAM is done by placing the row address of the cell on the address inputs of the memory chip and pulsing the row address strobe (ras). Actually 128 cells are addressed and refreshed by one row address. There are 128 rows that must be refreshed, therefore a refresh cycle must occur every 2ms/128 or15.6 us.

64K REFRESH CYCLE USING Z-80 TIMING **********

The Z80 CPU provides a time period for refresh cycles, (so that wait states are not needed) refresh pulse and a 7 bit refresh address after every instruction op code fetch (M1 cycle). The 64KDQ memory uses the timing and refresh pulses provided by the Z80 for its refresh cycles. There must be a connection between the Z80's refresh output and the 64KDQ refresh input (pin 66). the 64KDQ has its own refresh address counter inside the 3242 (IC U18). The refresh address provided by the Z80 CPU is ignored.

The refresh circuit (IC-U2) on the 64KDQ uses the falling edge of phi 2 (Z80 phi not) clock and refresh not to generate one 250 ns (at 4MHZ, 500 ns at 2 MHZ) ras refresh pulse. This pulse will coincide with T4 of the Z80's M1 cycle. At the end of the refresh cycle the on board refresh counter is incremented to the next row to be refreshed.

AUTOMATIC REFRESH CYCLES **********

The Z80 CPU does not always provide refresh cycles within the 15.6 us margin, therefore automatic refresh cycles must be inserted to maintain memory integrity. There are 3 cases where the Z80 may not provide refresh cycles. They are:

RESET STATE
WAIT STATE
DMA CYCLES

The 64KDQ treats reset and wait states in the same way. If a reset or wait state occurs, an interval counter (IC U11) clocked by phi 2 is enabled. If the counter reaches a count of 14, the PRDY line (S-100 pin72) is pulled low by an open collector driver (IC U4). A refresh cycle is done during count 15. At the end of the refresh cycle the PRDY line is released, the refresh address is incremented and the interval counter starts over at zero. This continues until the reset or wait state ends.

NOTE: XRDY (S-100 BUS pin 3) is not monitored by the 64KDQ. If XRDY is pulled low the 64K will forget everything in 2ms.

DMA CYCLE **********

No automatic refresh cycles can occur during a DMA cycle. The current temporary bus master must either provide refresh pulses that are synchronized with phi 2 and that look like the refresh pulses provided by the Z80, or it must release control of the bus back to the Z80 in less than 14 us (DMA cycles must be less than 14 us total). Temporary masters must also provide MREQ on S-100 bus pin 60.

INTERFACING THE 64KDQ TO A CPU **********

The 64KDQ comes jumpered from the factory to run with the XOR CPU. Other Z80 CPU cards must provide, besides the normal S-100 bus signals, memory request/not and refresh cycle not to run with the 64KDQ. These two signals are present on all Z80 CPU chips, but may not be brought out to the S-100 bus. If your CPU does not have these signals you need to find two spare non-inverting buffers and connect the inputs to the Z80 chip pin 19 (MREQ) and pin 28 (RFSH). The buffered MREQ should be connected to S100 bus pin 60. The buffered RFSH should be connected to S100 bus pin 66. Note: you should have good technical experience before attempting to add these modifications to your cpu.

FACTORY INSTALLED JUMPERS **********

JUMPER	INSTALLED	OPEN	FUNCTION IF INSTALLED
B-C		X	NO MEMORY MANAGEMENT
B-E		X	I/O PORT MEMORY MANAGE
S-T	X		ENABLE EXTENDED ADDRESS
F-H	X		ENABLE PHANTOM PIN 67
F-J	X		PULL UP PHANTOM
M-K	X		MREQ NO INVERSION
M-L		X	INVERT MREQ
P-N	X		USE MREQ TO START MEMORY CYCLE
P-R		X	USE MWRT+SMEMR TO START CYCLE
V-U	X		IGNORE A20,21,22,23 ADD LINES
V-W		X	USE ALL EXTENDED ADDRESS LINES
E8-E9	X		RESET I/O PORT LATCH ON PR75
E8-E10		X	RESET I/O PORT LATCH ON SLV 54
E16-E15	X		RFSH NO INVERSION
E16-E14		X	INVERT RFSH
E19-E18	X		RFSH ON PIN 66
E19-E17		X	RFSF ON PIN 66
E22-E21	X		NO INVERSION OF PHI TO COUNTER
E22-E20		X	INVERT PHI 2 TO AUTO RFSH
E23-E20	X		INVERT PHI TO RFSH CYCLE FLOP
E23-E21		X	NO INVERSION OF PHI 2 TO RFSH

64K - DQ PARTS LIST

PART NO.	DESCRIPTION	QTY.	PART NO.	DESCRIPTION	QTY.
I-0000-06	HTSNK-B	2	I-7000-10	ZEN+5.1	1
I-0000-13	NUT 4-40	2	I-7000-54	74S138	1
I-0000-27	SCREW 4-40	2	I-7400-15	4116-200NS	32
I-1000-22	S164KBD	1	I-7400-28	7438	1
I-2000-05	14PSOC	10	I-7400-50	74109	1
I-2000-06	16PSOC	39	I-7400-57	74161	1
I-2000-08	20PSOC	6	I-7400-71	74LS00	1
I-2000-10	28PSOC	1	I-7400-74	74LS04	1
I-3000-11	33 OHM RES	5	I-7400-79	74LS11	1
I-3000-28	10KSIP	3	I-7400-82	74LS85	1
I-3000-51	4DIPSW	1	I-7400-87	74LS74	1
I-3000-54	8DIPSW	2	I-7400-88	74LS85	2
I-3000-58	.1MF50VR	44	I-7401-07	74LS175	1
I-3000-59	1KRESC	1	I-7401-09	74LS244	1
I-3000-68	220RES	1	I-7401-10	74LS240	5
I-3000-81	33R-PAK	1	I-7401-20	3242	1
I-3001-17	4.7MF25VR	10	I-7401-22	74LS30	1
I-7000-02	REG+5	1	I-7401-39	PE21199	1
I-7000-03	REG+12	1			

TROUBLESHOOTING

If the memory board has been in service for some time and a problem with it is suspected, a memory test should be run.

There are many faults that can occur on a memory board. Not all errors can be found by running any single memory test. We have supplied two tests that were created from years of manufacturing experience.

The first test ('MEMTEST') when run in its fundamental mode (executed under CP/M by typing M (cr) then (cr) (cr) in response to the start and stop questions,) will calculate the system size and begin a typical pattern of tests to uncover the most common problems first and the most uncommon ones last.

Typing a 'P' along with the address in the address field will PAUSE the test program after the memory fill passes. After the operator has waited an appropriate amount of time he may hit (cr) to continue the test. This feature will test for the existence of Phantom-bits. These are memory cells that change after being left un-accessed for a period of time. Initiating the test with M<sp>R<cr> will exclude the address and data tests and drop immediately into the random numbers test.

A second test called 'WORM' is designed to find memory cells that cannot stand rapid cycle time demands placed on them by some of the Z80 block move and math routines. While these chips will pass all standard memory tests for hours on end, they randomly fail during program execution time for seemingly unexplained reasons. The reason is that there is a difference between a chips ACCESS time and its CYCLE time. We generally only rate a memory board by its access time, (i.e. 450ns or 250ns.)

Worm starts itself at the load address and relocates itself repeatedly, reporting its current location periodically. It 'tests' by simply moving itself and constantly doing instruction fetches. A RAM failure is evidenced by the program crashing. The last reported address on the CRT should be interpreted to be the bank in which the errant chip resides. Binary replacing of chips, one half at a time, watching to see when the problem moves to the new bank, will uncover the bad device.

S100 BUS LINE ASSIGNMENTS

X=Recommended lines to terminate

LINE	NAME	TYPE	POLARITY	LINE	NAME	TYPE	POLARITY
1	+8	BUS		51	+8	B	
2	+15	B		52	-15	B	
3	XRDY	B	P	53	GND	B	
4	V10	SLAVE	N	54	SLV/CLR	B	N
5	V11	S	N	55	DMA0	M	N
6	V12	S	N	56	DMA1	M	N
7	V13	S	N	57	DMA2	M	N
8	V14	S	N	58	SXTRQ	M	N
9	V15	S	N	59	A19	M	N
10	V16	S	N	60	SIXTN	S	N
11	V17	S	N	61	A20	M	P
12	NMI	S	N	62	A21	M	P
13	PWRFAIL	B	N	63	A22	M	P
14	DMA3	MASTER	N	64	A23	M	P
15	A18	M	P	65	MRQ	TTL	
16	A16	M	P	66	REFRESH	TTL	
17	A17	M	P	67	PHANTOM	B	N
18X	STAT DSB	M	N	68X	MWRITE	B	P
19	C/C DSB	M	N	69	RFU		
20	GND	B		70	GND		
21	RFU			71	RFU		
22X	ADD DSB	M	N	72	pRDY	S	P
23X	DO DSB	M	N	73	pINT	S	N
24X	O2	B	P	74	pHOLD	M	N
25X	pSTVAL	M	N	75	pRESET	B	N
26X	pHLDA	M	P	76X	pSYNC	M	P
27	RFU			77	PWR	M	N
28	RFU			78X	pDBIN	M	P
29X	A5	M	P	79X	A0	M	P
30X	A4	M	P	80X	A1	M	P
31X	A3	M	P	81X	A2	M	P
32X	A15	M	P	82X	A6	M	P
33X	A12	M	P	83X	A7	M	P
34X	A9	M	P	84X	A8	M	P
35X	DO1/D1	M,M/S	P	85X	A13	M	P
36X	DO0/D0	M,M/S	P	86X	A14	M	P
37X	A10	M	P	87X	A11	M	P
38X	DO4/D4	M,M/S	P	88X	DO2/D2	M,M/S	P
39X	DO5/D5	M,M/S	P	89X	DO3/D3	M,M/S	P
40X	DO6/D6	M,M/S	P	90X	DO7/D7	M,M/S	P
41X	D12/D11	S,M/S	P	91X	D14/D12	S,M/S	P
42X	D13/D11	S,M/S	P	92X	D15/D13	S,M/S	P
43X	D17/D15	S,M/S	P	93X	D16/D14	S,M/S	P
44X	sM1	M	P	94X	D11/D9	S,M/S	P
45X	sOUT	M	P	95X	D10/D8	S,M/S	P
46X	sINP	M	P	96X	sINTA	M	P
47X	sMEMR	M	P	97X	sWO	M	N
48	sHLTA	M	P	98	ERROR	M/S	N
49X	CLOCK	B	N	99	POC		N
50	GND	B		100	GND	B	

RFU = Reserved for future use.

PIN NO.	SIGNAL	POLARITY	DESCRIPTION
1	+8(B)		INSTANTANEOUS MIN GREATER THAN 7 VOLTS BUT LESS THAN 25 VOLTS AVERAGE LESS THAN 11 VOLTS
2	+16(B)		INSTANTANEOUS MIN GREATER THAN 14.5 VOLTS BUT LESS THAN 35 V AVERAGE LESS THAN 21.5 VOLTS
3	XRDY	P	ONE OF TWO READY INPUTS TO THE CURRENT BUS MASTER. THE BUS IS READY WHEN BOTH THESE INPUTS ARE TRUE.
4	$\overline{\text{V10}}$(S)	N	VECTORED INTERRUPT LINE 0
5	$\overline{\text{V11}}$(S)	N	VECTORED INTERRUPT LINE 1
6	$\overline{\text{V12}}$(S)	N	VECTORED INTERRUPT LINE 2
7	$\overline{\text{V13}}$(S)	N	VECTORED INTERRUPT LINE 3
8	$\overline{\text{V14}}$(S)	N	VECTORED INTERRUPT LINE 4
9	$\overline{\text{V15}}$(S)	N	VECTORED INTERRUPT LINE 5
10	$\overline{\text{V16}}$(S)	N	VECTORED INTERRUPT LINE 6
11	$\overline{\text{V17}}$(S)	N	VECTORED INTERRUPT LINE 7
12	$\overline{\text{NMI}}$ (S)	N	NON-MASKABLE INTERRUPT
13	$\overline{\text{PWR FAIL}}$(B)	N	POWER FAIL BUS INTERRUPT
14	$\overline{\text{DMA3}}$ (M)	N	DIRECT MEMORY ACCESS DEVICE ADDRESS AT BIT 3
15	A18 (M)	P	EXTENDED ADDRESS BIT 18
16	A16 (M)	P	EXTENDED ADDRESS BIT 16
17	A17 (M)	P	EXTENDED ADDRESS BIT 17
18	$\overline{\text{STAT DSB}}$ (M)	N	THE CONTROL SIGNAL TO DISABLE THE 9 STATUS SIGNALS
19	$\overline{\text{C/C DSB}}$ (M)	N	THE CONTROL SIGNAL TO DISABLE THE COMMAND/CONTROL SIGNALS.

PIN NO.	SIGNAL	POLARITY	DESCRIPTION
20	GROUND		
21	RFU		
22	$\overline{\text{ADD DSB}}$ (M)	N	THE CONTROL SIGNAL TO DISABLE THE 16 ADDRESS SIGNALS
23	$\overline{\text{DO/DSB}}$(M)	N	THE CONTROL SIGNAL TO DISABLE THE 8 DATA OUTPUT SIGNALS
24	ø 2 (B)	P	THE MASTER BUS TIMING SIGNAL
25	$\overline{\text{pSTVAL}}$ (M)	N	STATUS VALID STROBE
26	pHLDA (M)	P	A COMMAND CONTROL SIGNAL USED WITH PHOLD TO COORDINATE BUS MASTER TRANSFER OPERATIONS
27	RFU		
28	RFU		
29	A5 (M)	P	ADDRESS BIT 5
30	A4 (M)	P	ADDRESS BIT 4
31	A3 (M)	P	ADDRESS BIT 3
32	A15 (M)	P	ADDRESS BIT 15 (MOST SIGNIFICANT FOR NON-EXTENDED ADDRESSING)
33	A12 (M)	P	ADDRESS BIT 12
34	A9 (M)	P	ADDRESS BIT 9
35	DO1 (M)/DATA 1	P	DATA OUT BIT 1
36	DOO (M)/DATA 0	P	DATA OUT BIT 0
37	A10 (M)	P	ADDRESS BIT 10
38	DO4 (M)/DATA4	P	DATA OUT BIT 4, BI DATA 4
39	DO5 (M)/DATA5	P	DATA OUT BIT 5, BI DATA 5
40	DO6 (M)/DATA6	P	DATA OUT BIT 6, BI DATA 6
41	D12 (S)/DATA10	P	DATA IN BIT 2, BI DATA 10

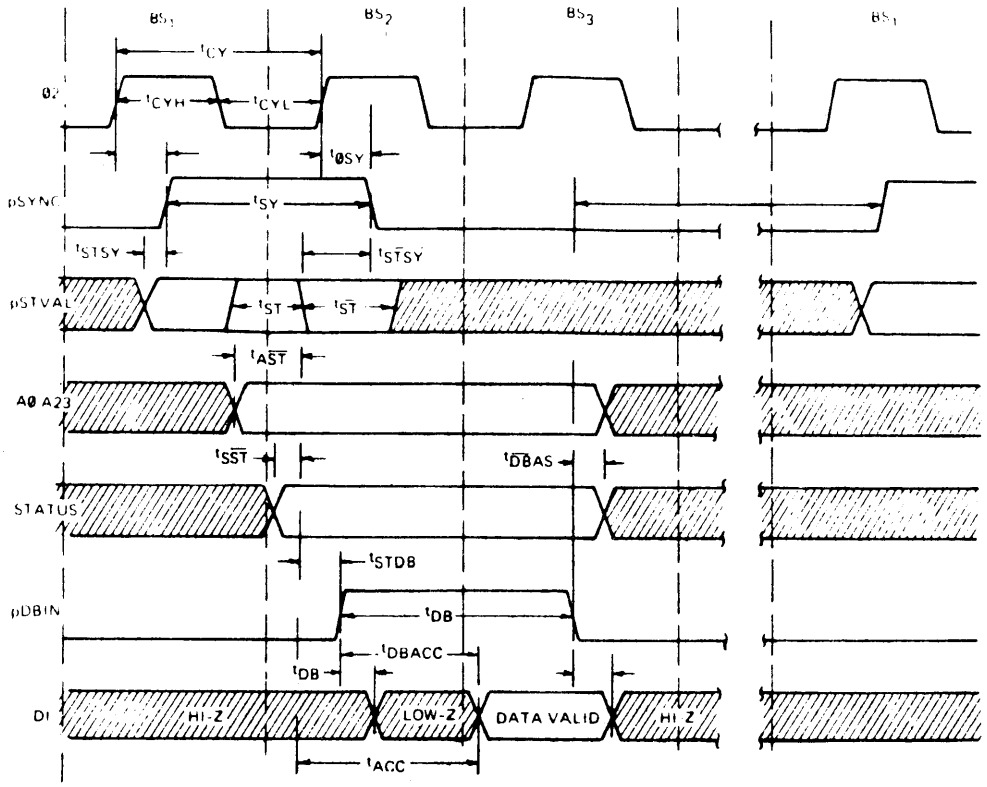
PIN NO.	SIGNAL	POLARITY	DESCRIPTION
42	D13 (S)/DATA11	P	DATA IN BIT 3 BI DATA 11
43	D17 (S)/DATA15	P	DATA IN BIT 7 BI DATA 15
44	sM1 (M)	P	THE STATUS SIGNAL WHICH INDICATES THAT THE CURRENT CYCLE IS IN OP CODE FETCH.
45	sOUT (M)	P	THE STATUS SIGNAL IDENTIFING THE DATA TRANSFER BUS CYCLE OF AN OUT INSTRUCTION
46	sINP (M)	P	THE STATUS SIGNAL IDENTIFING THE DATA TRANSFER BUS CYCLE OF AN INPUT INSTRUCTION
47	sMEMR (M)	P	THE STATUS SIGNAL IDENTIFING BUS CYCLES WHICH TRANSFER DATA FROM MEMORY TO A BUS MASTER WHICH ARE NOT INTERRUPT ACKNOWLEDGE INSTRUCTION FETCH CYCLES.
48	sHLTA (M)		THE STATUS SIGNAL WHICH ACKNOWLEDGES THAT A HLT INST HAS BEEN EXECUTED
49	$\overline{\text{CLOCK}}$ (B)		2MHZ (2%) 40-60 DUTY CYCLE. NOT REQUIRED TO BE SYNCHRONOUS WITH ANY OTHER BUS SIGNAL.
50	GROUND		
51	+8 VOLTS (B)		SEE PIN 1
52	- 16 VOLTS (B)		MAX LESS THAN -14.5 MIN GREATER THAN -35 AVERAGE MIN LESS THAN -21.5
53	GROUND		
54	$\overline{\text{SLAVE CLR}}$ (B)	N	RESET BUS SLAVES. MUST BE ACTIVE WITH POC AND MAY ALSO BE GENERATED BY EXT SIG.
55	$\overline{\text{DMA0}}$ (M)	N	DMA DEVICE ADDRESS BIT 0
56	$\overline{\text{DMA1}}$ (M)	N	DMA DEVICE ADDRESS BIT 1
57	$\overline{\text{DMA2}}$ (M)	N	DMA DEVICE ADDRESS BIT 2

PIN NO.	SIGNAL	POLARITY	DESCRIPTION
58	$\overline{\text{SXTRQ}}$ (M)	N	THE STATUS SIGNAL WHICH REQUESTS 16 BIT SLAVES TO ASSERT SIXTN
59	A19	P	EXTENDED ADDRESS BIT 19
60	$\overline{\text{SIXTN}}$ (S)	N	THE SIGNAL GENERATED BY 16 BIT SLAVES IN RESPONSE TO THE 16 BIT REQUEST SIG SXTRQ
61	A20 (M)	P	EXTENDED ADDRESS BIT 20
62	A21 (M)	P	EXTENDED ADDRESS BIT 21
63	A22 (M)	P	EXTENDED ADDRESS BIT 22
64	A23 (M)	P	EXTENDED ADDRESS BIT 23
65	MRQ		MEMORY REQUEST
66	REFRESH		REFRESH CYCLE
67	$\overline{\text{PHANTOM}}$ (B)	N	A BUS SIGNAL WHICH DISABLES NORMAL SLAVE DEVICES AND ENABLES PHANTOM SLAVES PRIMARILY USED FOR BOOT-STRAPPING SYSTEMS WITHOUT HARDWARE FRONT PANELS
68	MWRITE(B)	P	PWR+sOUT THIS SIGNAL MUST FOLLOW PWR BY NOT NOTE THAN 30 NS.
69	RFU		
70	GND		
71	RFU		
72	PRDY(S)	P	SEE PIN 3
73	$\overline{\text{PINT}}$ (S)	P	THE PRIMARY INTERRUPT REQUEST BUS SIGNAL
74	pHOLD (M)	N	THE COMMAND CONTROL SIG USED WITH PHLDA TO COORDINATE BUS MASTER TRANSFER OPERATIONS.

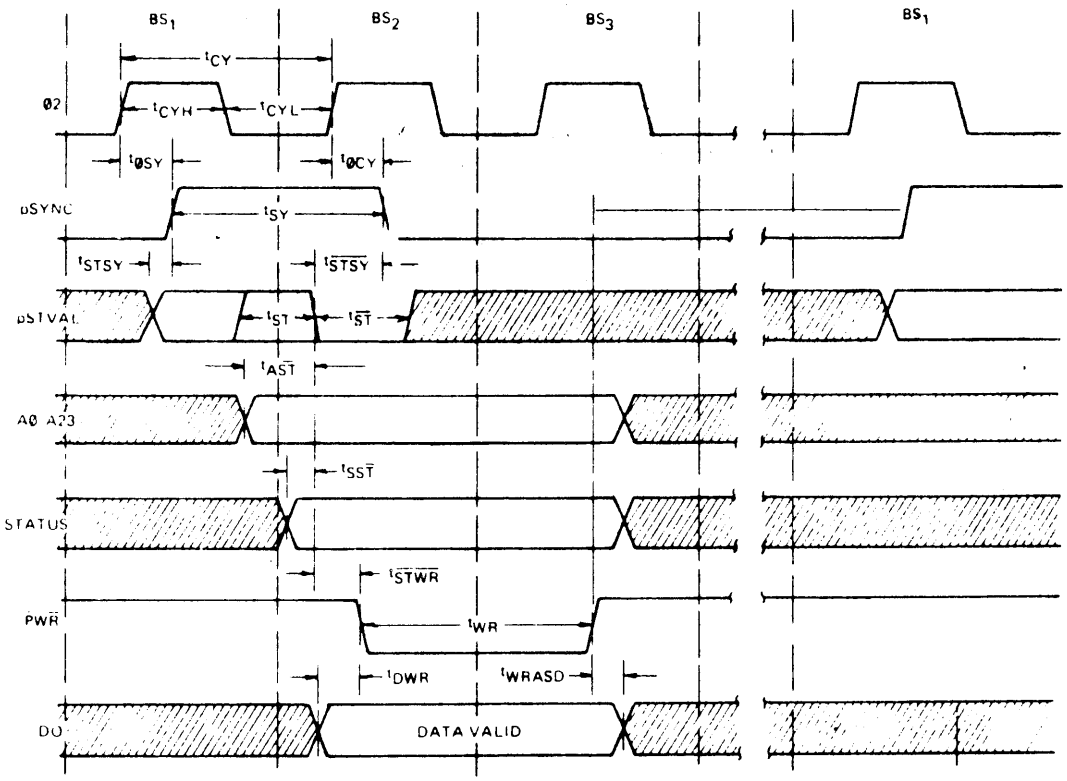
PIN NO.	SIGNAL	POLARITY	DESCRIPTION
75	$\overline{\text{pRESET}}$ (M)	N	THE RESET SIGNAL TO RESET BUS MASTER DEVICES. THIS SIGNAL MUST BE ACTIVE WITH POC AND MAY ALSO BE GENERATED BY EXTERNAL MEANS.
76	pSYNC (M)	P	THE COMMAND CONTROL SIGNAL IDENTIFING BS
77	$\overline{\text{pWR}}$ (M)	N	THE COMMAND CONTROL SIGNAL SIGNIFING THE PRESENCE OF VALID DATA ON DO BUS OR DATA BUS
78	pDBIN(M)	P	THE COMMAND CONTROL SIGNAL THAT REQUESTS DATA ON THE D1 BUS OR DATA BUS FROM THE CURRENTLY ADDRESSED SLAVE
79	A0 (M)	P	ADDRESS BIT 0
80	A1 (M)	P	ADDRESS BIT 1
81	A2 (M)	P	ADDRESS BIT 2
82	A6 (M)	P	ADDRESS BIT 6
83	A7 (M)	P	ADDRESS BIT 7
84	A8 (M)	P	ADDRESS BIT 8
85	A13 (M)	P	ADDRESS BIT 13
86	A14 (M)	P	ADDRESS BIT 14
87	A11 (M)	P	ADDRESS BIT 11
88	DO2 (M)DATA2	P	DATA OUT 2 BIDATA 2
89	DO3 (M)DATA3	P	DATA OUT 3 BIDATA 3
90	DO7 (M)DATA7	P	DATA OUT 7 BIDATA 7
91	D14 (M)DATA12	P	DATA IN BIT 4 BIDATA BIT 12
92	D15 (S)DATA13	P	DATA IN BIT 5 BIDATA BIT 13
93	D16 (S)DATA14	P	DATA IN BIT 6 BIDATA BIT 14
94	D11 (S)DATA9	P	DATA IN BIT 1 BIDATA BIT 9

PIN NO.	SIGNAL	POLARITY	DESCRIPTION
95	D10 (S)DATA8	P	DATA IN BIT 0 BIDATA BIT 8
96	sINTA (M)	P	THE STATUS SIGNAL IDENTIFING THE BUS INPUT CYCLE THAT MAY FOLLOW AN ACCEPTED INTERRUPT REQUEST PRESENTED ON pINT.
97	$\overline{\text{sWO}}$ (M)	N	THE STATUS SIGNAL IDENTIFING A BUS CYCLE WHICH TRANSFERS DATA FROM A BUS MASTER TO A SLAVE
98	$\overline{\text{ERROR}}$ (S)	N	THE BUS STATUS SIGNAL SIGNIFING AN ERROR CONDITION DURING A PRESENT OR PREVIOUS BUS CYCLE.
99	$\overline{\text{POC}}$(B)	N	THE POWER ON CLEAR SIGNAL FOR ALL BUS DEVICES. WHEN THIS SIGNAL GOES LOW, IT MUST STAY LOW FOR AT LEAST 3 BUS STATES.
100	GROUND		

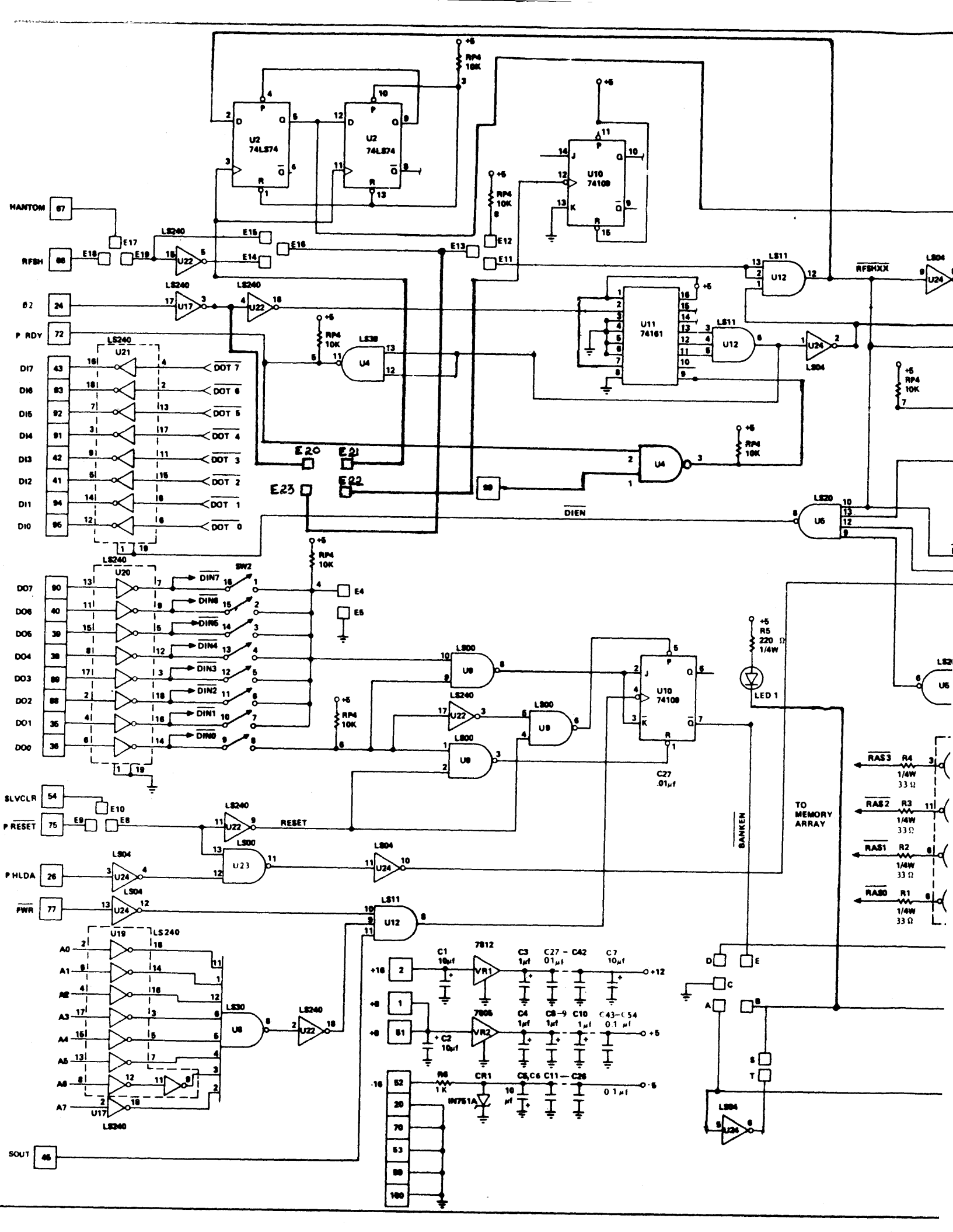
READ CYCLE

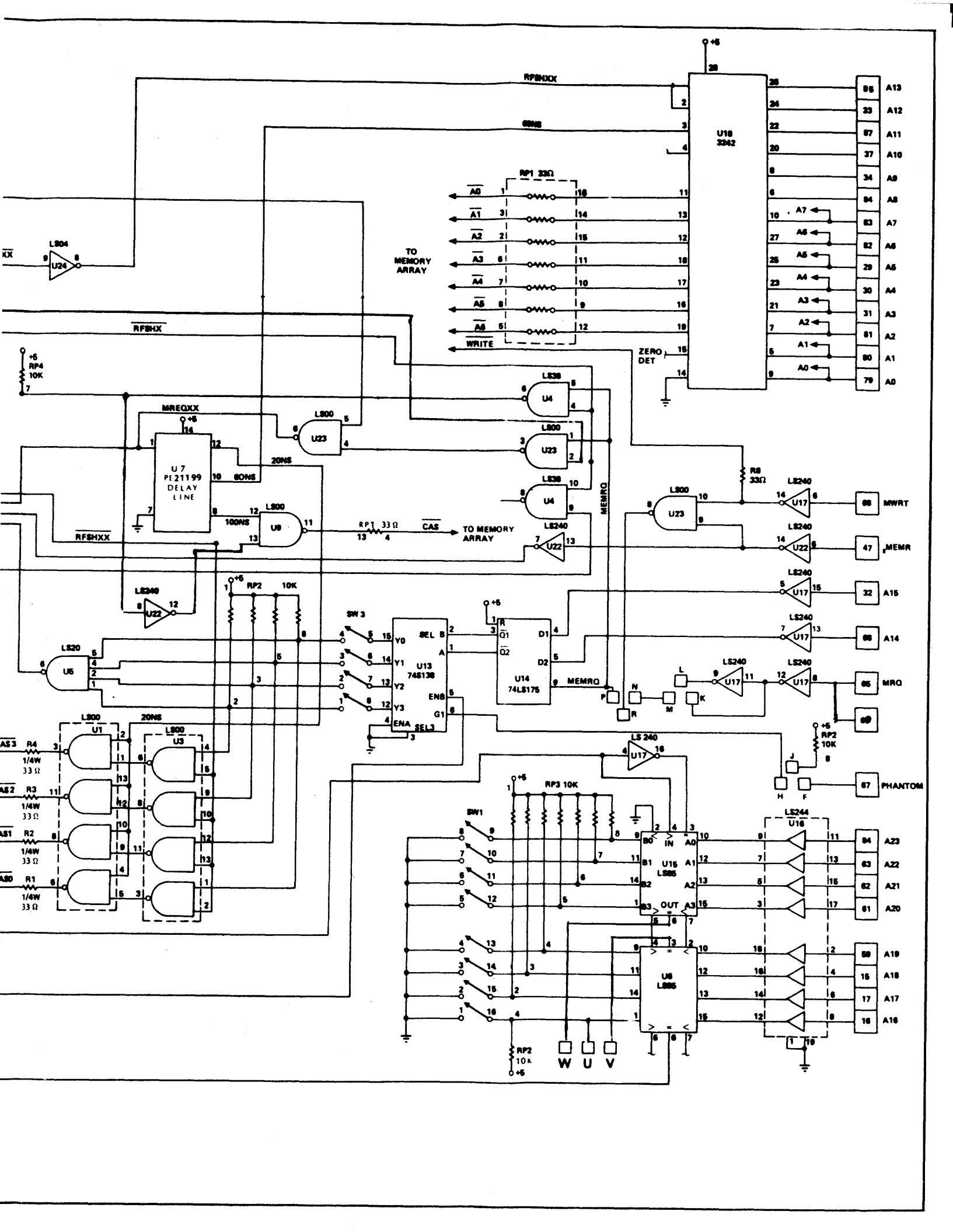


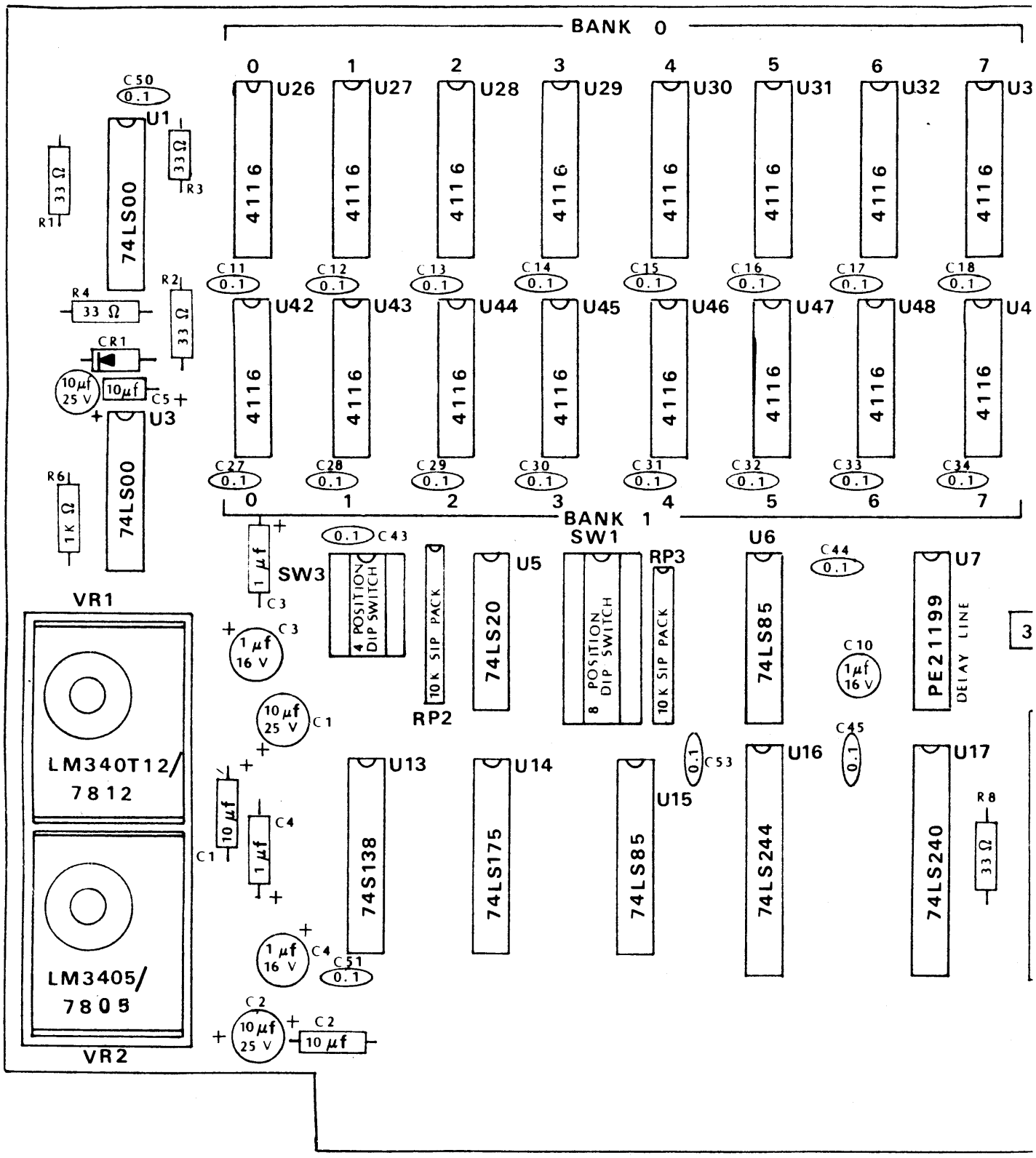
WRITE CYCLE

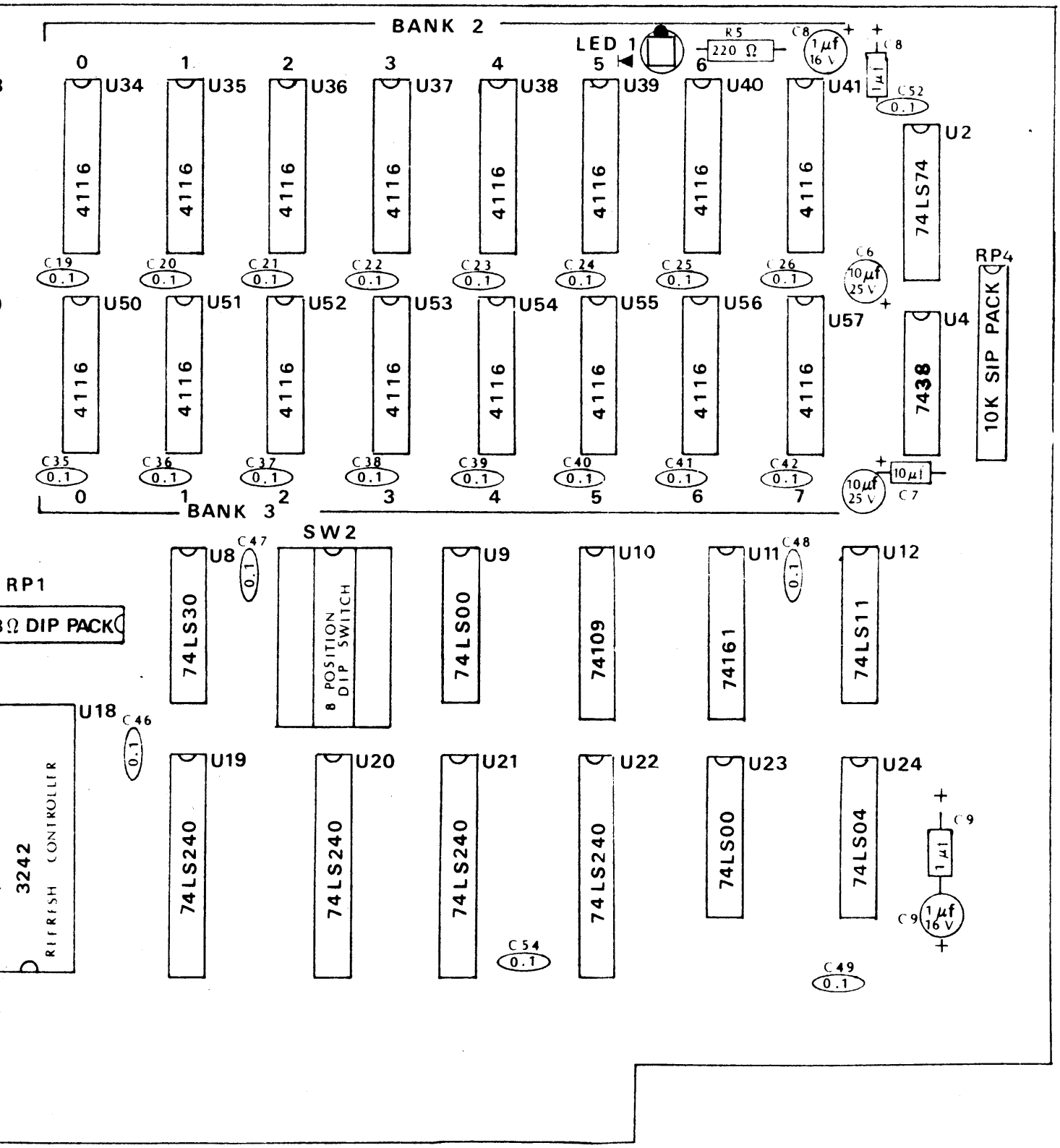


Timing Diagrams


U2 74LS74
U2 74LS74
U10 74109
U11 74161
U10 74109
U10 74109
HANTOM
RFSH
Ø2
P RDY
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
SLVCLR
P RESET
P HLDA
PWR
SOUT
A0
A1
A2
A3
A4
A5
A6
A7
DIEN
RFSHXX
RESET
BANKEN
TO MEMORY ARRAY
LED 1
RAS3
RAS2
RAS1
RAS0
7812
7805
IN751A


RFSHXX
80NS
U18
3242
RP1 33Ω
TO MEMORY ARRAY
WRITE
ZERO DET
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
LS04
U24
RFSHX
RP4 10K
MREQXX
U7
PE21199
DELAY LINE
20NS
80NS
100NS
U9
RP1 33Ω
CAS
TO MEMORY ARRAY
RFSHXX
LS38
U4
LS00
U23
MEMRQ
RS 33Ω
LS240
U17
U22
MWRT
MEMR
A15
A14
MRQ
LS20
U5
RP2 10K
SW 3
U13
74S138
U14
74LS175
MEMRQ
LS 240
PHANTOM
U1
U3
R4 1/4W 33Ω
R3 1/4W 33Ω
R2 1/4W 33Ω
R1 1/4W 33Ω
SW1
RP3 10K
LS244
U16
U15
LS85
U8
LS85
A23
A22
A21
A20
A19
A18
A17
A16
W
U
V


BANK 0
0
1
2
3
4
5
6
7
U26
U27
U28
U29
U30
U31
U32
U3
4116
C50
0.1
U1
74LS00
33 Ω
R1
R3
R2
R4
CR1
10µf 25 V
10µf
C5
U3
R6
1K Ω
VR1
LM340T12/
7812
LM3405/
7805
VR2
C11
C12
C13
C14
C15
C16
C17
C18
U42
U43
U44
U45
U46
U47
U48
U4
C27
C28
C29
C30
C31
C32
C33
C34
BANK 1
SW3
4 POSITION DIP SWITCH
1 µf
C3
16 V
10 µf 25 V
C1
10 µf
C4
74S138
U13
74LS175
U14
74LS85
U15
74LS20
U5
RP2
10K SIP PACK
SW1
8 POSITION DIP SWITCH
RP3
U6
74LS85
C44
C10
U7
PE21199
DELAY LINE
C53
C45
U16
74LS244
U17
74LS240
R8
C51
C2
3


BANK 2
LED 1
R5
220 Ω
C8
1 µf
16 V
C8
1 µ1
C52
0.1
U2
74LS74
RP4
10K SIP PACK
C6
10 µf
25 V
U4
7438
10 µf
C7
0 1 2 3 4 5 6
BANK 3
U34 U35 U36 U37 U38 U39 U40 U41
U50 U51 U52 U53 U54 U55 U56 U57
4116
C19 C20 C21 C22 C23 C24 C25 C26
C35 C36 C37 C38 C39 C40 C41 C42
0.1
SW2
8 POSITION DIP SWITCH
C47
C48
U8 74LS30
U9 74LS00
U10 74109
U11 74161
U12 74LS11
RP1
Ω DIP PACK
U18
3242
REFRESH CONTROLLER
C46
U19 74LS240
U20 74LS240
U21 74LS240
U22 74LS240
U23 74LS00
U24 74LS04
C54
C49
C9
1 µ1
C9
1 µf
16 V